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# MS-7591

uATXVersion: 0A

**CPU:** BloomField Processors In LGA1366 Package.

## System Chipset:

Intel Tylersburg I/O Hub 36S (North Bridge)

Intel ICH10R (South Bridge)

## On Board Devices:

CLOCK Gen -- ICS 9LPRS113

LPC Super I/O -- Fintek F71882F

LAN --BCM5784M

HD Audio Codec -- ALC888S

1394 Controller -- VT6315N

eSATA -- SIL3132

## Main Memory:

3-Channel A / B / C DDR-III \*6


## Expansion Slots:

PCI EXPRESS X16 SLOT \*2

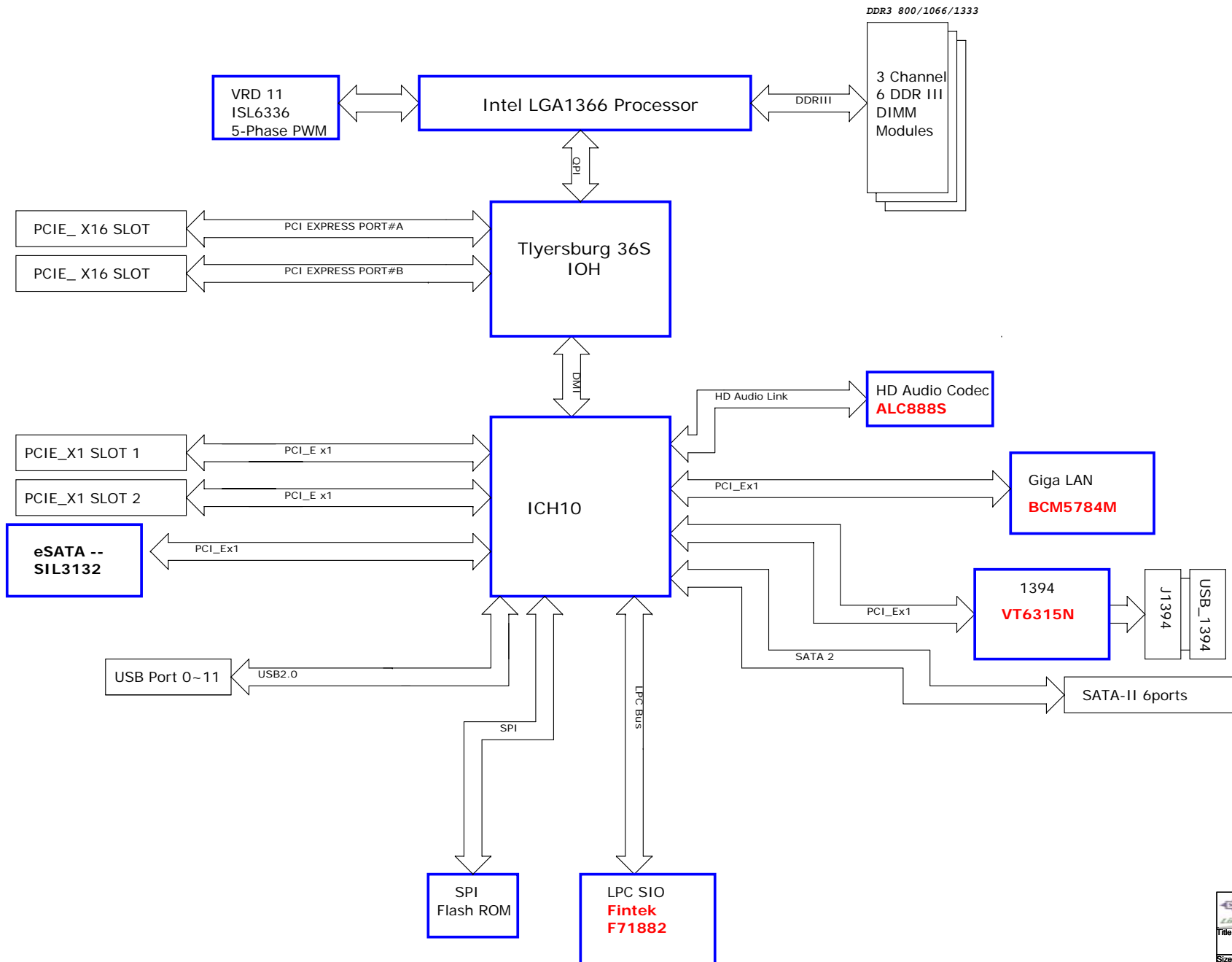
PCI EXPRESS X1 SLOT \* 2

**PWM:** VR11.1 Intersil ISL6336 (5 Phases)

# DELL DEIMOS

 <b>MICRO-START INT'L CO.,LTD.</b>		
Title <b>COVER SHEET</b>		
Size	Document Number	Rev
Custom	<b>DELL Deimos</b>	<b>0A</b>
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## Block Diagram



9 DATA\_A[0..63] &lt;&lt;&gt;

10 DATA\_B[0..63] &lt;&lt;&gt;

11 DATA\_C[0..63] &lt;&lt;&gt;

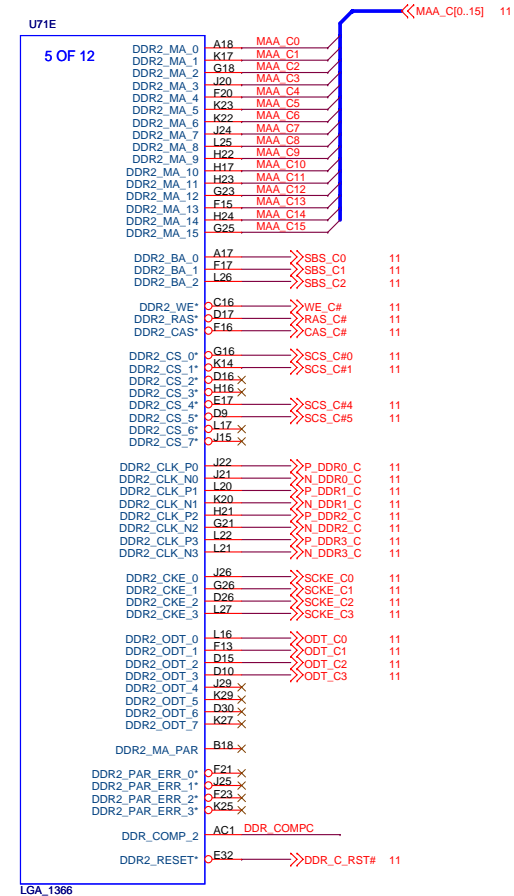
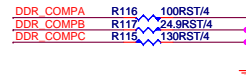
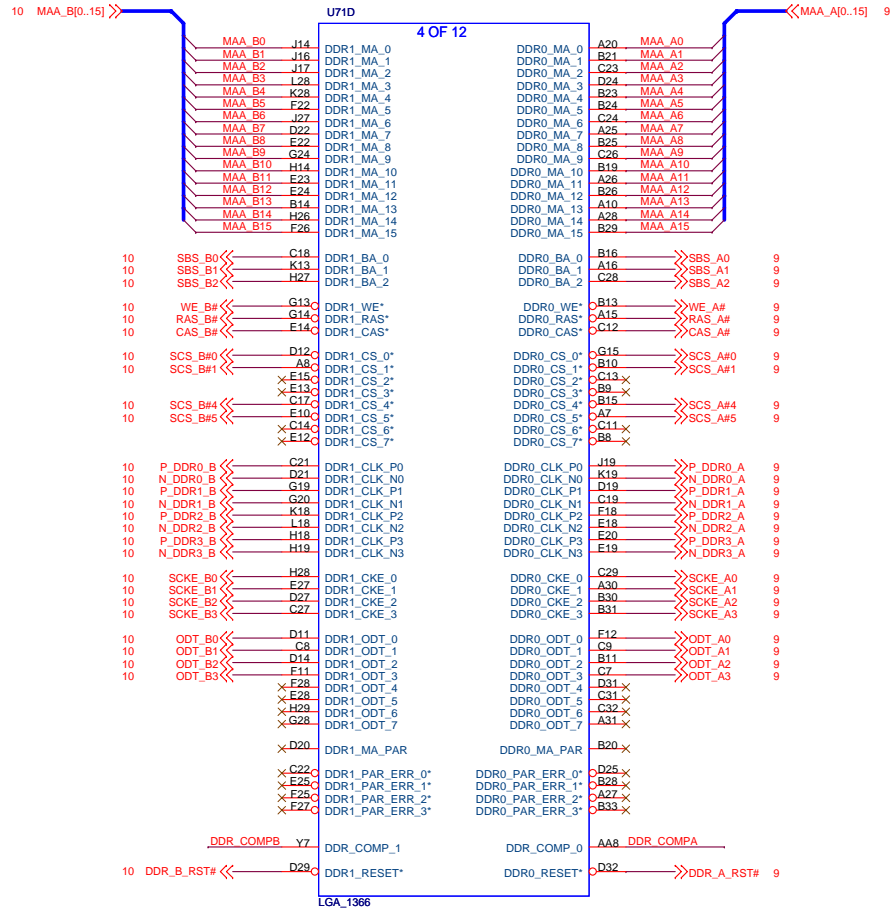
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DATA A2	R43	DDR0_DQ_2		L41	<<>	DQS_A1	9		
DATA A3	R42	DDR0_DQ_3	DDR0_DQS_P1	M41	<<>	DQS_A#1	9		
DATA A4	W40	DDR0_DQ_4	DDR0_DQS_N1						
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DATA A6	U41	DDR0_DQ_6	DDR0_DQS_P2	G41	<<>	DQS_A#2	9		
DATA A7	T42	DDR0_DQ_7	DDR0_DQS_N2						
DATA A8	N41	DDR0_DQ_8		B39	<<>	DQS_A3	9		
DATA A9	N43	DDR0_DQ_9	DDR0_DQS_P3	B40	<<>	DQS_A#3	9		
DATA A10	K42	DDR0_DQ_10	DDR0_DQS_N3						
DATA A11	K43	DDR0_DQ_11		E3	<<>	DQS_A4	9		
DATA A12	P42	DDR0_DQ_12	DDR0_DQS_P4	E4	<<>	DQS_A#4	9		
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DATA A21	J41	DDR0_DQ_21	DDR0_DQS_P7	W1	<<>	DQS_A#7	9		
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DATA A24	D40	DDR0_DQ_24	DDR0_DQS_P8	D35	<<>				
DATA A25	C41	DDR0_DQ_25	DDR0_DQS_N8						
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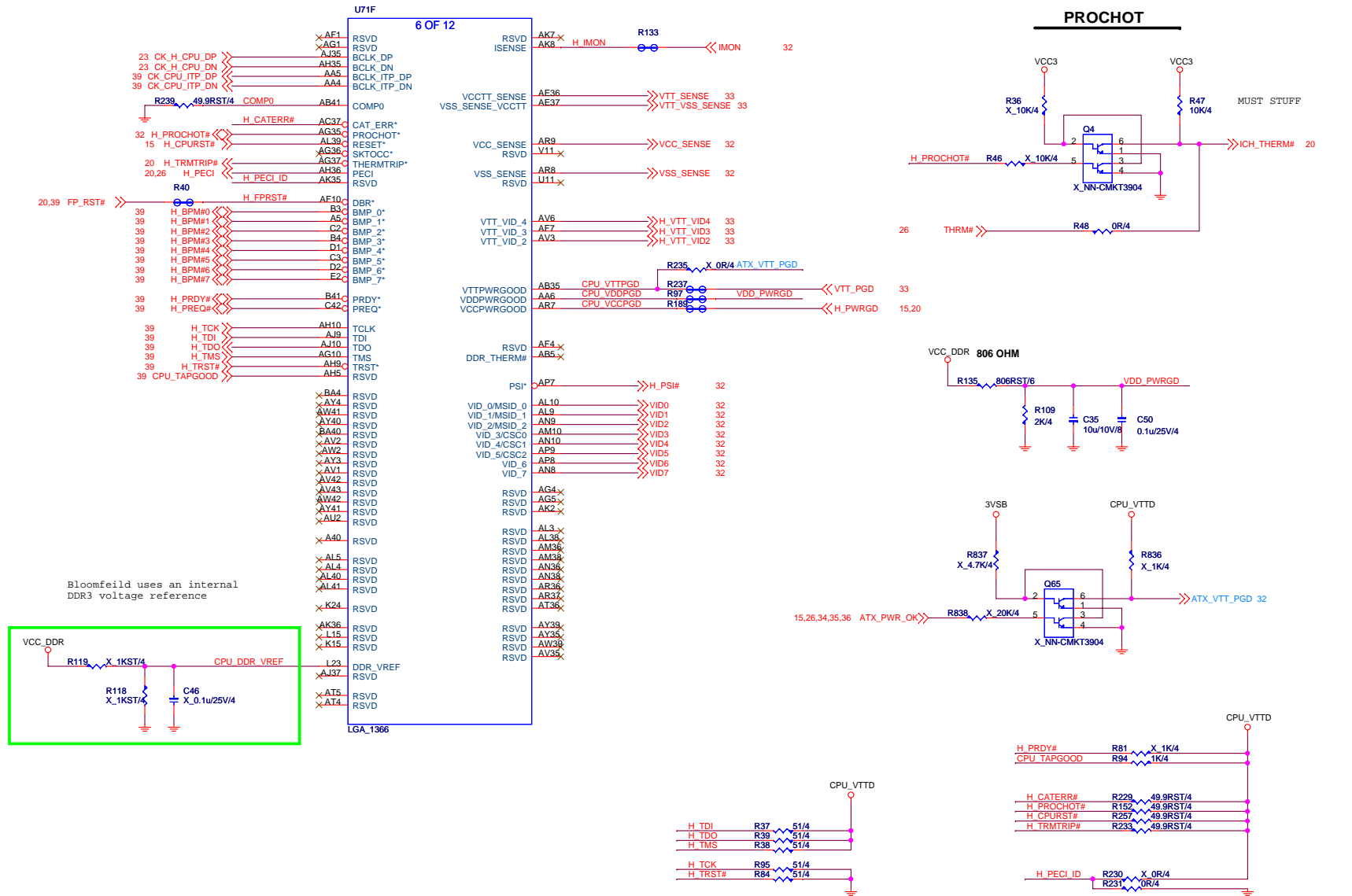
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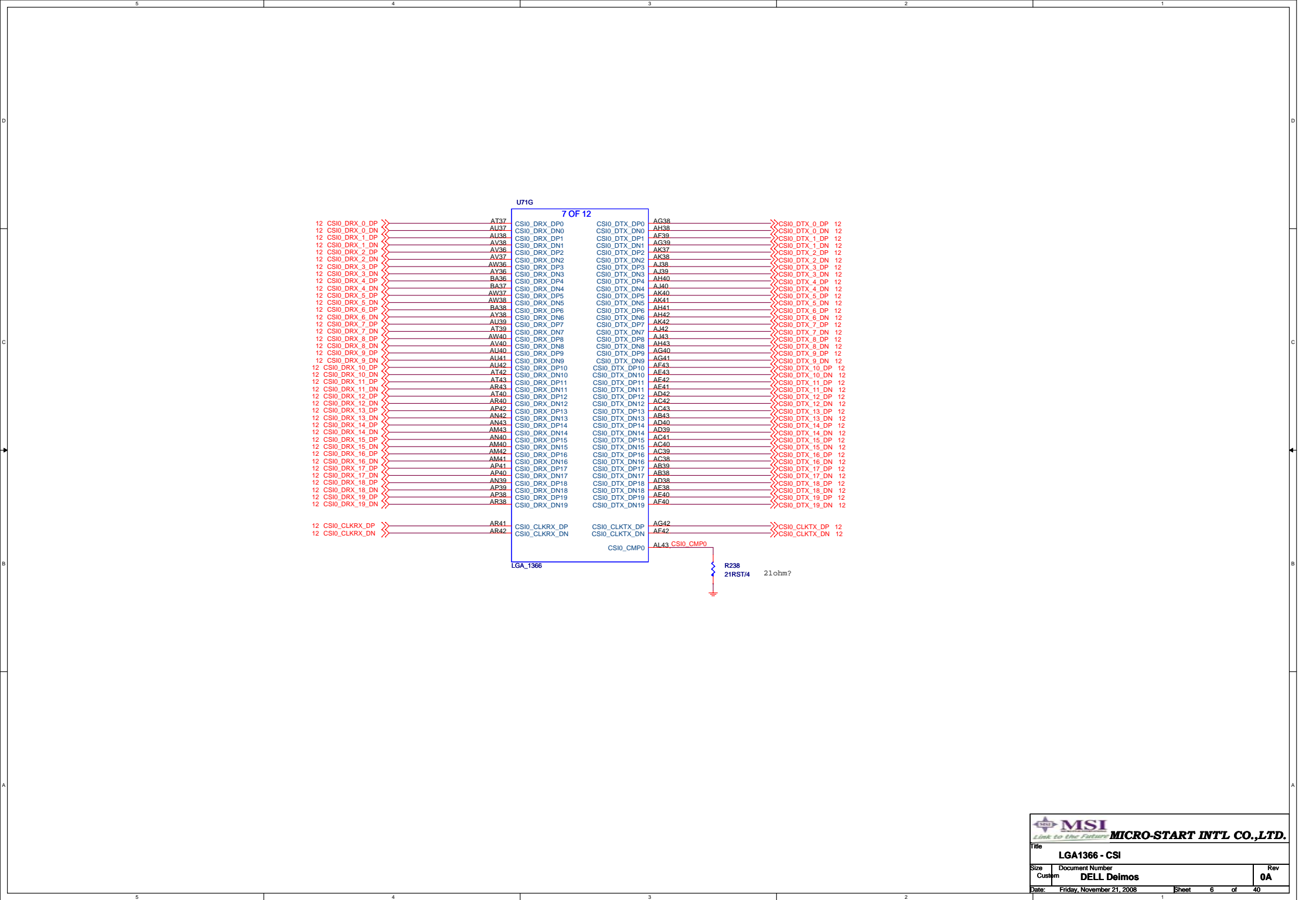
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DATA B3	Y34	DDR1_DQ_3	DDR1_DQS_P1	R37	<<>	DQS_B#1	10		
DATA B4	AA35	DDR1_DQ_4	DDR1_DQS_N1						
DATA B5	AB36	DDR1_DQ_5		L35	<<>	DQS_B2	10		
DATA B6	Y35	DDR1_DQ_6	DDR1_DQS_P2	L36	<<>	DQS_B#2	10		
DATA B7	Y40	DDR1_DQ_7	DDR1_DQS_N2						
DATA B8	P34	DDR1_DQ_8		L30	<<>	DQS_B3	10		
DATA B9	P35	DDR1_DQ_9	DDR1_DQS_P3	L31	<<>	DQS_B#3	10		
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DATA B11	N39	DDR1_DQ_11		E7	<<>	DQS_B4	10		
DATA B12	R34	DDR1_DQ_12	DDR1_DQS_P4	D7	<<>	DQS_B#4	10		
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DATA B18	K35	DDR1_DQ_18	DDR1_DQS_P6	L5	<<>	DQS_B#6	10		
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DATA B20	N34	DDR1_DQ_20		Y8	<<>	DQS_B7	10		
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DATA B23	K36	DDR1_DQ_23		G33	<<>				
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DATA B42	G4	DDR1_DQ_42	DDR1_DQS_P14	J7	<<>				
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DATA B44	G8	DDR1_DQ_44		M5	<<>				
DATA B45	H8	DDR1_DQ_45	DDR1_DQS_P15	M4	<<>				
DATA B46	G5	DDR1_DQ_46	DDR1_DQS_N15						
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DATA B53	M6	DDR1_DQ_53							
DATA B54	R8	DDR1_DQ_54							
DATA B55	R7	DDR1_DQ_55							
DATA B56	W6	DDR1_DQ_56							
DATA B57	W7	DDR1_DQ_57							
DATA B58	Y10	DDR1_DQ_58							
DATA B59	W10	DDR1_DQ_59							
DATA B60	V9	DDR1_DQ_60							
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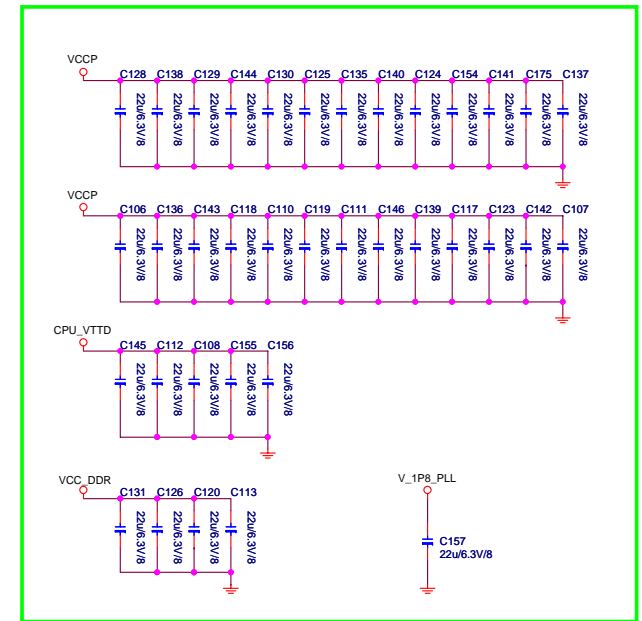
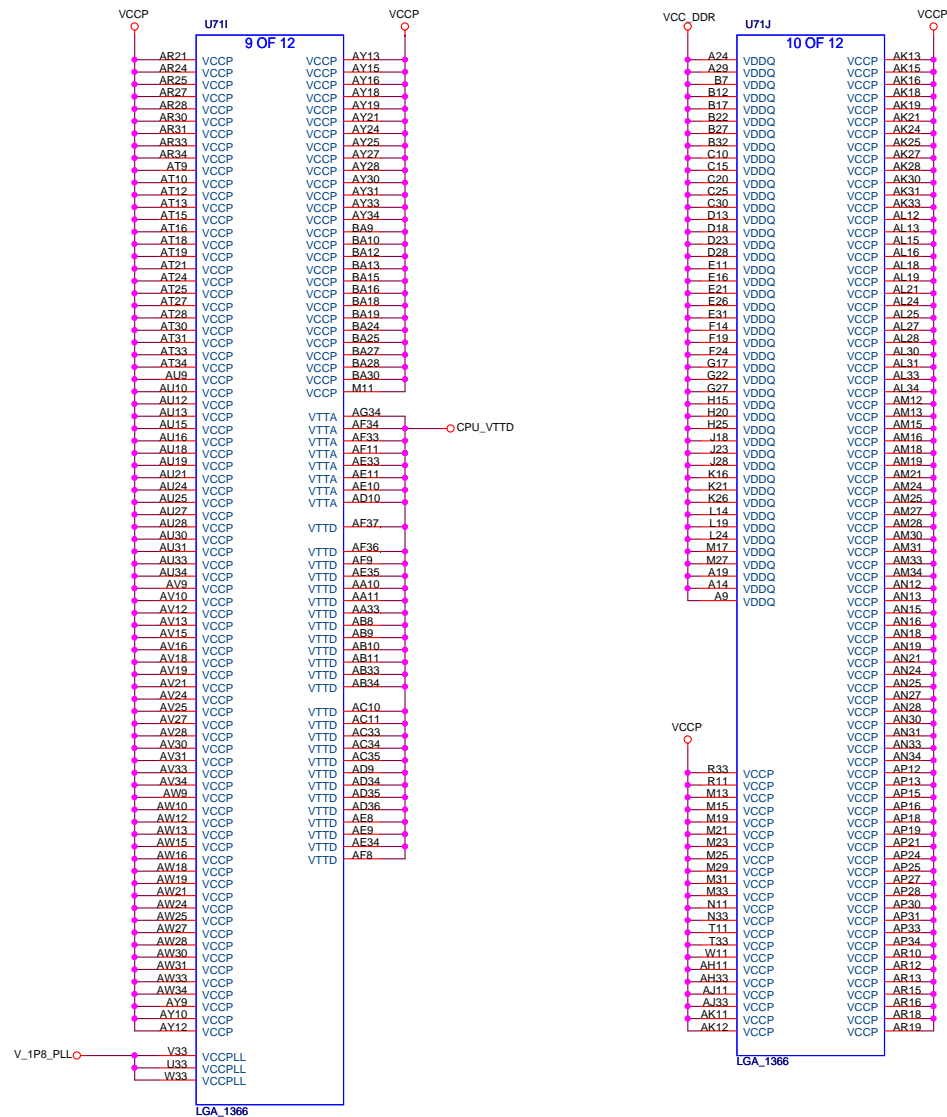
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DATA C5	V34	DDR2_DQ_5							
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DATA C7	V38	DDR2_DQ_7	DDR2_DQS_N2	K39		DQS_C#2	11		
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DATA C9	U39	DDR2_DQ_9	DDR2_DQS_P3	E39		DQS_C3	11		
DATA C10	R39	DDR2_DQ_10	DDR2_DQS_N3	E40		DQS_C#3	11		
DATA C11	T36	DDR2_DQ_11							
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DATA C13	V39	DDR2_DQ_13	DDR2_DQS_N4	J9		DQS_C#4	11		
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DATA C22	L40	DDR2_DQ_22	DDR2_DQS_N7						
DATA C23	K38	DDR2_DQ_23		G29					
DATA C24	G40	DDR2_DQ_24	DDR2_DQS_P8	G30					
DATA C25	F40	DDR2_DQ_25	DDR2_DQS_N8						
DATA C26	J37	DDR2_DQ_26		U35					
DATA C27	H37	DDR2_DQ_27	DDR2_DQS_P9	T38					
DATA C28	H39	DDR2_DQ_28	DDR2_DQS_N9						
DATA C29	G39	DDR2_DQ_29							
DATA C30	F38	DDR2_DQ_30	DDR2_DQS_P10	U40					
DATA C31	F38	DDR2_DQ_31	DDR2_DQS_N10	T40					
DATA C32	K12	DDR2_DQ_32							
DATA C33	J12	DDR2_DQ_33	DDR2_DQS_P11	M38					
DATA C34	H13	DDR2_DQ_34	DDR2_DQS_N11	L38					
DATA C35	L13	DDR2_DQ_35							
DATA C36	G11	DDR2_DQ_36	DDR2_DQS_P12	H38					
DATA C37	G10	DDR2_DQ_37	DDR2_DQS_N12	G38					
DATA C38	H12	DDR2_DQ_38							
DATA C39	L12	DDR2_DQ_39	DDR2_DQS_P13	H11					
DATA C40	L10	DDR2_DQ_40	DDR2_DQS_N13	J11					
DATA C41	K10	DDR2_DQ_41							
DATA C42	M9	DDR2_DQ_42	DDR2_DQS_P14	K9					
DATA C43	N9	DDR2_DQ_43	DDR2_DQS_N14	K8					
DATA C44	L11	DDR2_DQ_44							
DATA C45	M10	DDR2_DQ_45	DDR2_DQS_P15	N4					
DATA C46	L8	DDR2_DQ_46	DDR2_DQS_N15	P4					
DATA C47	M8	DDR2_DQ_47							
DATA C48	F7	DDR2_DQ_48	DDR2_DQS_P16	V6					
DATA C49	N6	DDR2_DQ_49	DDR2_DQS_N16	V7					
DATA C50	P9	DDR2_DQ_50							
DATA C51	P10	DDR2_DQ_51	DDR2_DQS_P17	H31					
DATA C52	N8	DDR2_DQ_52	DDR2_DQS_N17	G31					
DATA C53	N7	DDR2_DQ_53							
DATA C54	R10	DDR2_DQ_54							
DATA C55	R9	DDR2_DQ_55							
DATA C56	U5	DDR2_DQ_56							
DATA C57	U6	DDR2_DQ_57							
DATA C58	T10	DDR2_DQ_58							
DATA C59	U10	DDR2_DQ_59							
DATA C60	T6	DDR2_DQ_60							
DATA C61	T7	DDR2_DQ_61							
DATA C62	V8	DDR2_DQ_62							
DATA C63	U9	DDR2_DQ_63							
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✕F33		DDR2_ECC_1							
✕E29		DDR2_ECC_2							
✕E30		DDR2_ECC_3							
✕J31		DDR2_ECC_4							
✕J30		DDR2_ECC_5							
✕F31		DDR2_ECC_6							
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INSIDE CPU SOCKET





# DIMM1 / CHANNEL A0

# DIMM2 / CHANNEL A1

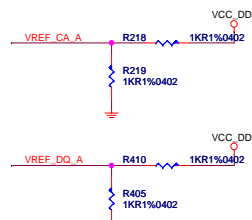
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Close to the DIMM VTT\_DDR Pin

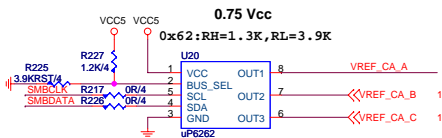
DDR3

DDR3

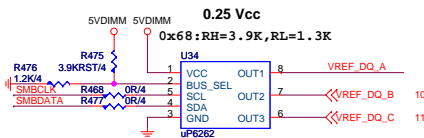
## UPI VOLTAGE CONSOLE



0.75 Vcc



0.25 Vcc



10,11 SMBCLK\_DDR

10,11 SMBDATA\_DDR

15,20,23,24,25,32,33,34,39

15,20,23,24,25,32,33,34,39

10,11 SMBCLK\_DDR

10,11 SMBDATA\_DDR

15,20,23,24,25,32,33,34,39

15,20,23,24,25,32,33,34,39

**MSI**  
Link to the Future

**MICRO-START INT'L CO.,LTD.**

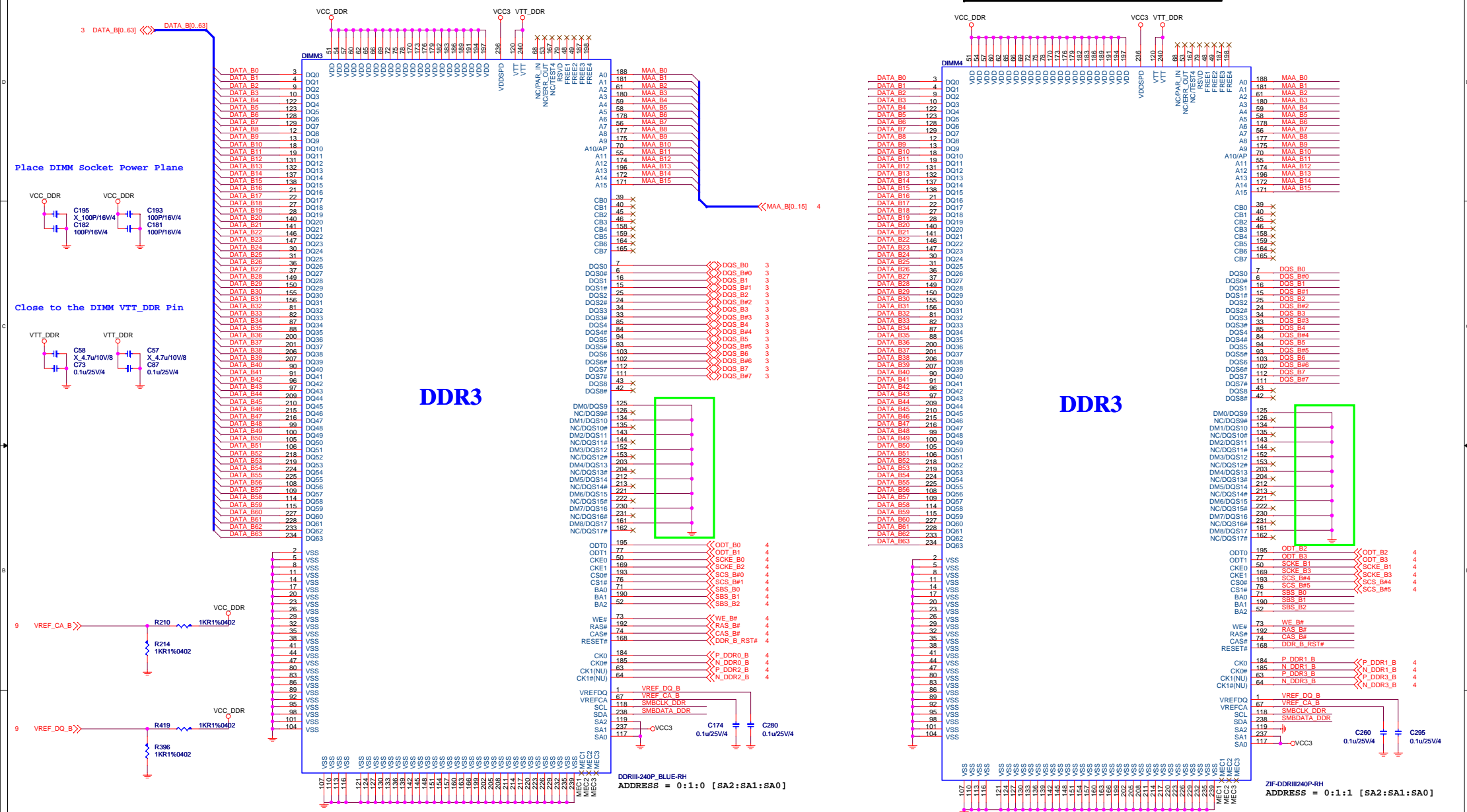
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Size: **Custom** Document Number: **DELL Delmos** Rev: **0A**

Date: **Friday, November 21, 2008** Sheet: **9** of **40**

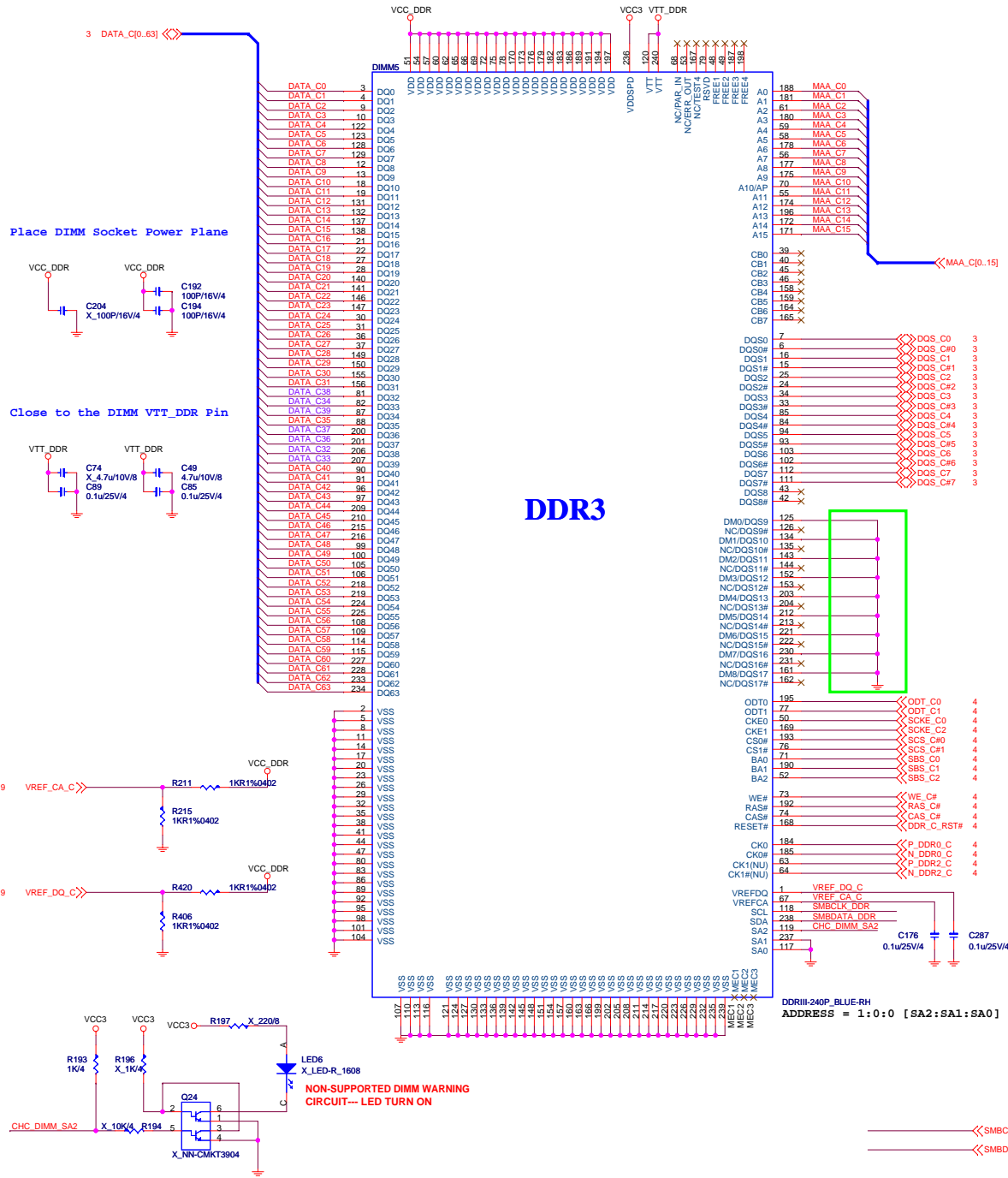
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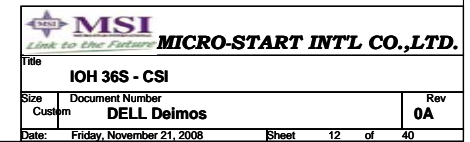
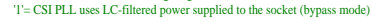
# DIMM4 / CHANNEL B1

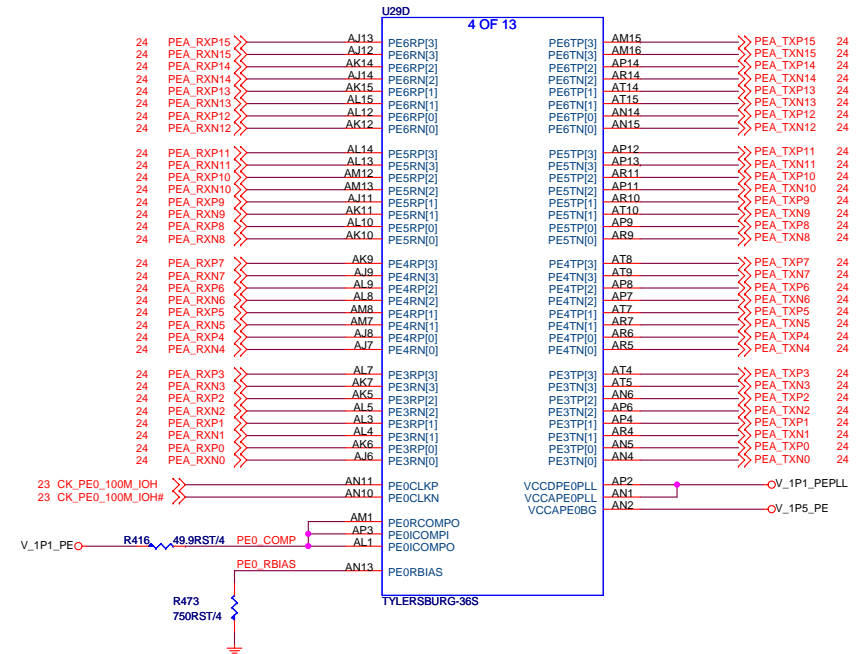
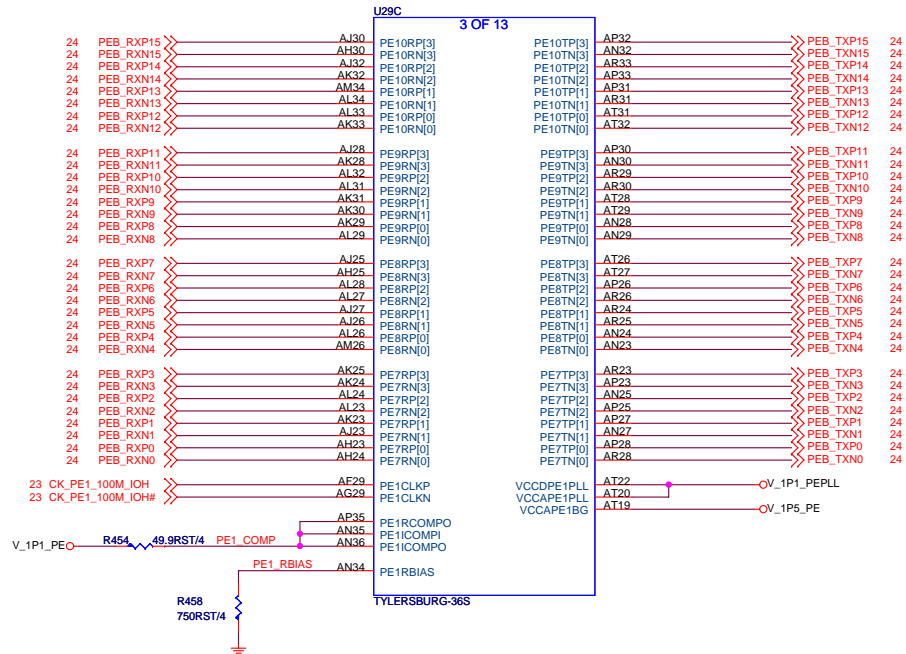


# DIMM5 / CHANNEL C0

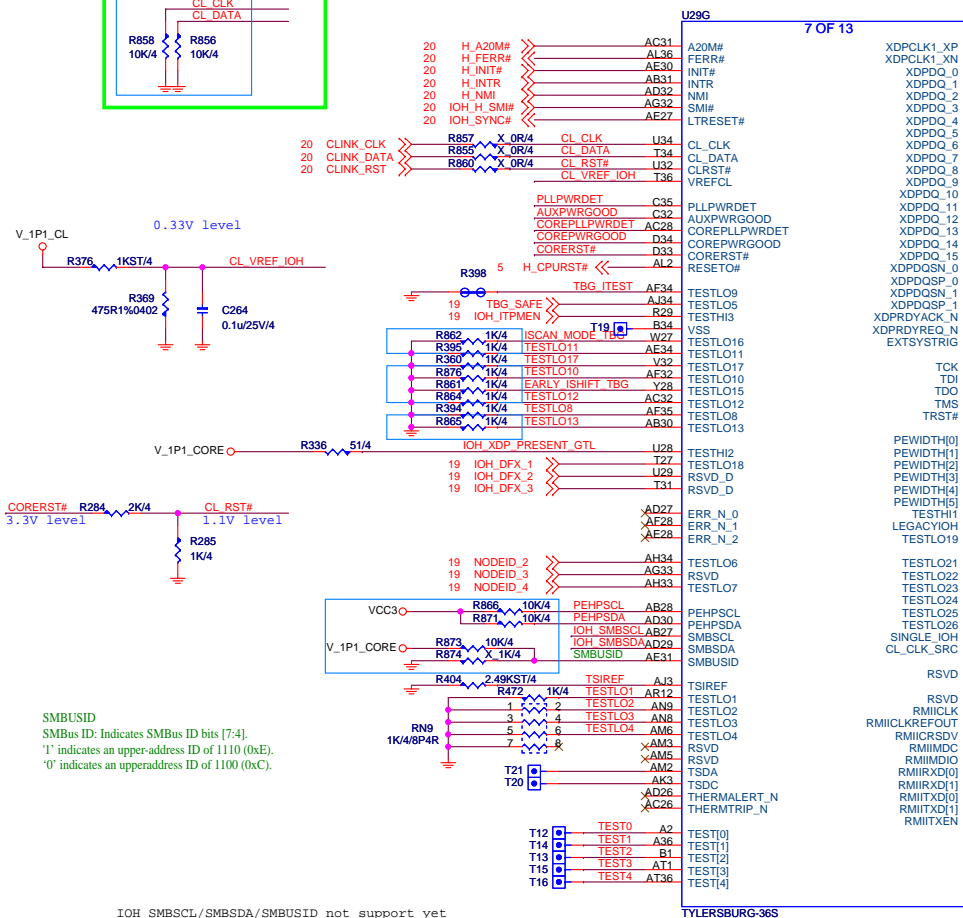
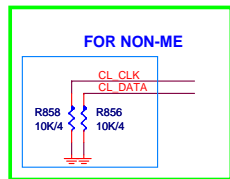
# DIMM6 / CHANNEL C1



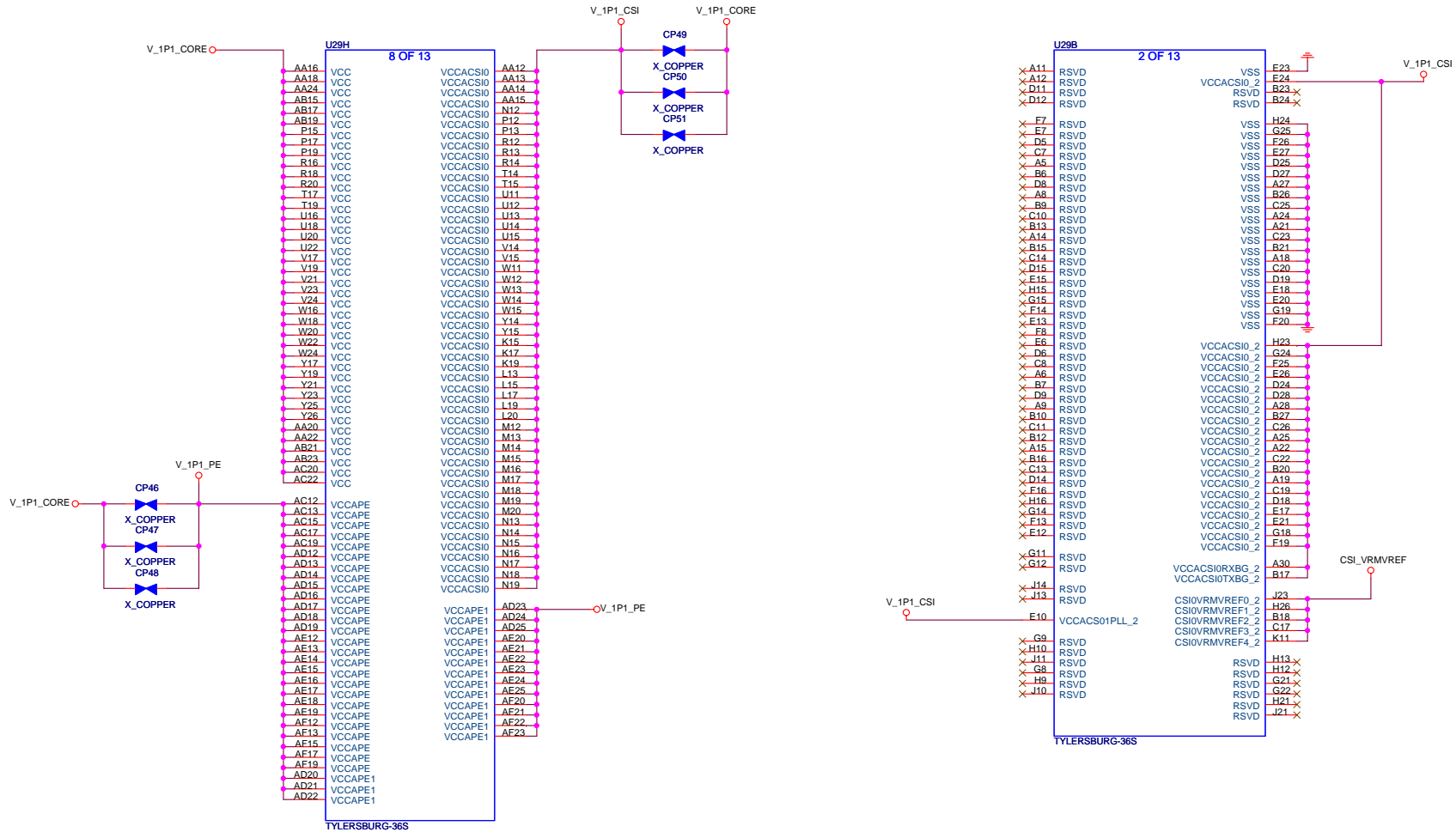




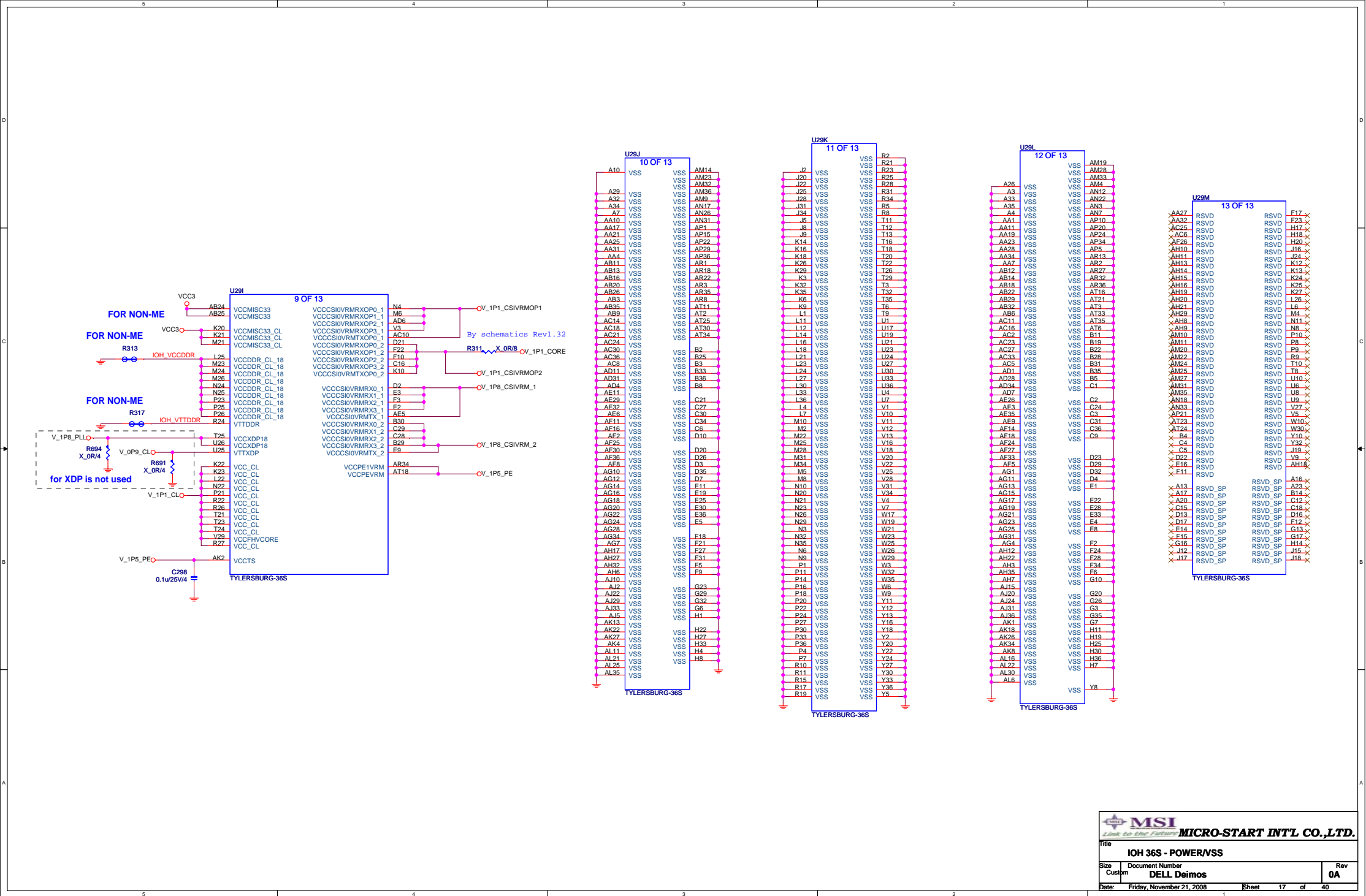












V\_1P1\_CORE REPLACE WITH V\_1P1\_VCCA

0.7A???

V\_1P1\_CORE

10mA $\times$ 2=20mA

V\_1P1\_CSIBG = CSIBG\_RX+CSIBG\_TX

35mA $\times$ 4=140mA

V\_1P1\_PEPLL = PEPLLA+PEPLLD

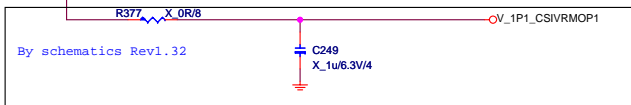
? mA

V\_1P1\_CSIPLL = CSI\_PLL

(120mA $\times$ 4+60mA)??=0.54A ?????

V\_1P1\_CSIVRMOP1 = CSIVRMOP\_RX[1:4]+CSIVRMOP\_TX1

Reduce leakage out through PCI Express (PEPLL) signals from IOH



1.08A

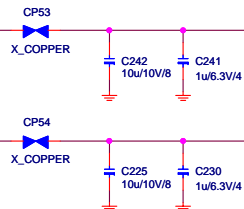
V\_1P8\_PLL

120mA $\times$ 4+60mA=0.54A

V\_1P1\_CSIVRM\_1 = CSIVRM\_RX\_1+CSIVRM1\_TX\_1

120mA $\times$ 4+60mA=0.54A

V\_1P1\_CSIVRM\_2 = CSIVRM\_RX\_2+CSIVRM1\_TX\_2



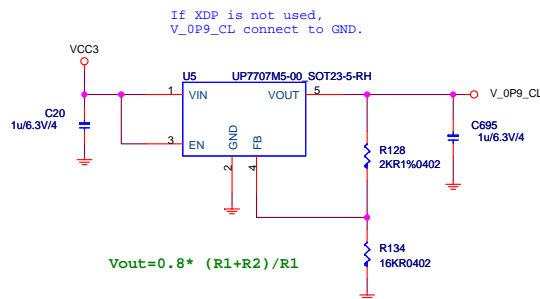
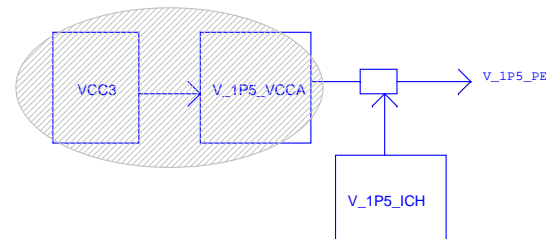
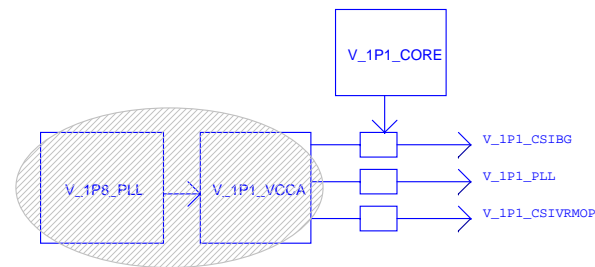
186.3mA+?

V\_1P5\_ICH

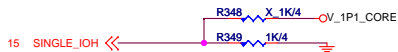
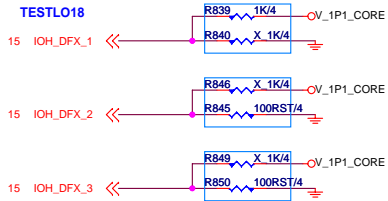
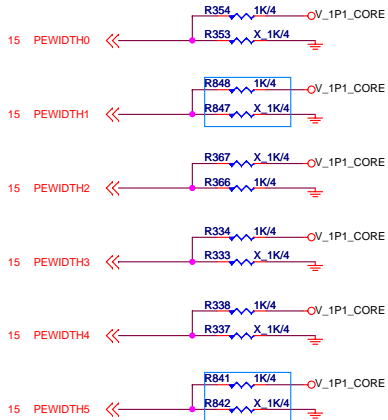
V\_1P5\_ICH REPLACE WITH V\_1P5\_VCCA

92mA $\times$ 2+1.15mA $\times$ 2+=186.3mA+?

V\_1P5\_PE = PEVRM+PEBG0+PEBG1+VCCTS



PEWIDTH0-5  
PCIE Link Width Select  
"111011" = 2x16  
"101111" = 4x8  
"011111" = Wait On Bios

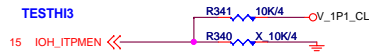
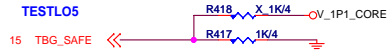
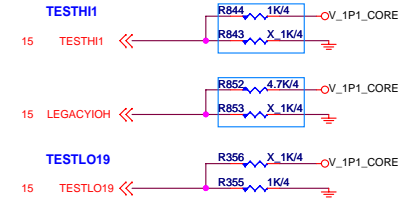
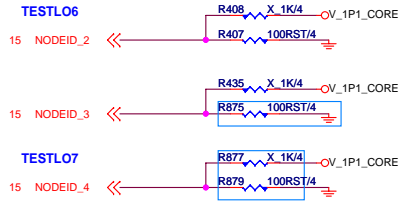


#### NON-ME FUNCTION

VCCADDRPLL and ME\_CLK\_SRC  
pins must be tied to VSS as well

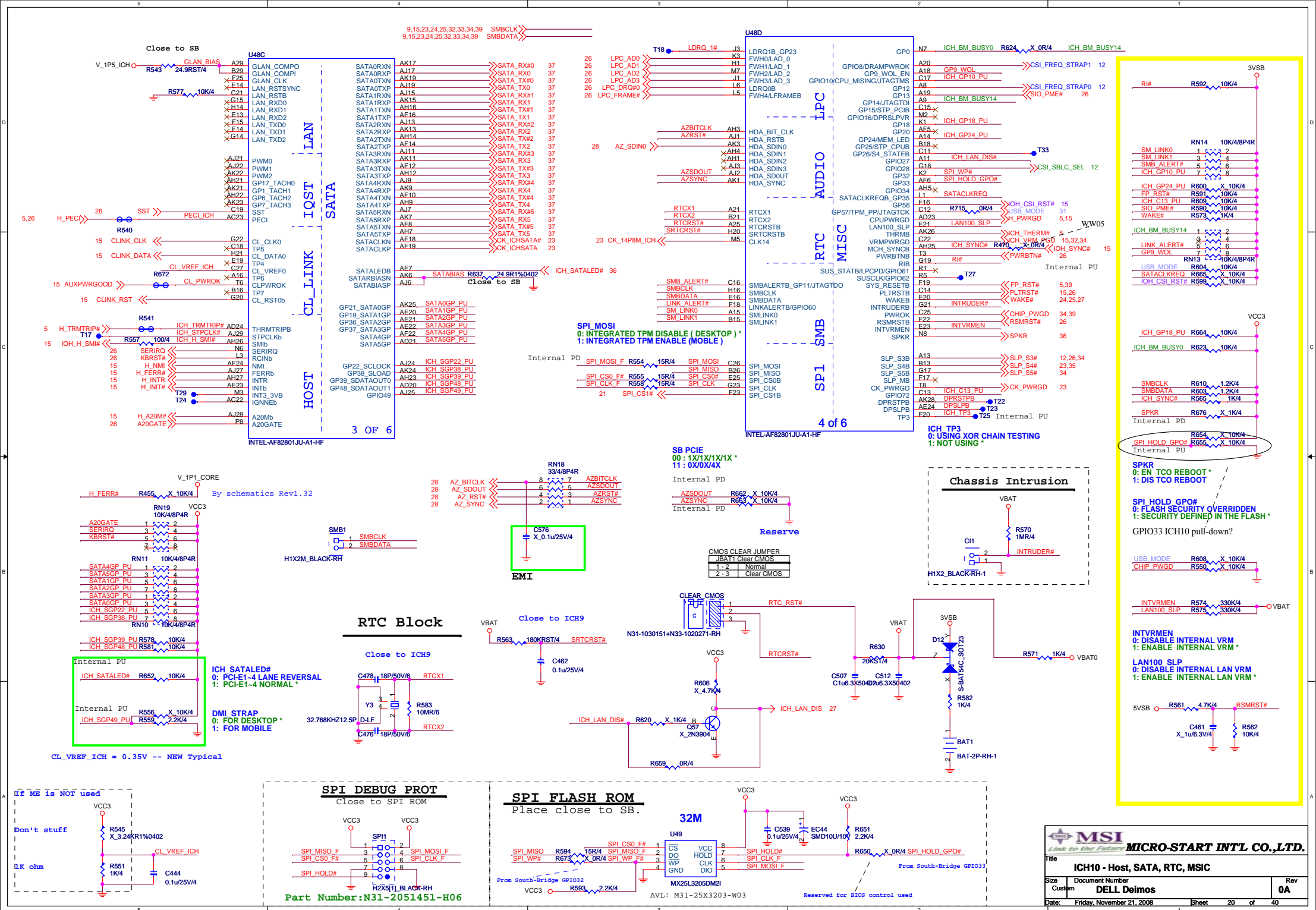
NODEID\_3\_TBG  
For dual TBG IOH configuration,  
it indicates which CSI port is connected to  
the other IOH.  
"0": CSI0  
"1": CSI1

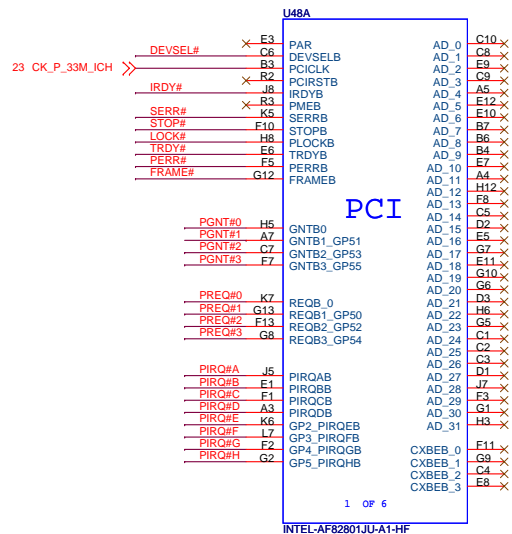
LEGACYIOH  
Used to determine legacy or non-legacy selection:  
"1": Legacy IOH  
"0": Non-legacy IOH



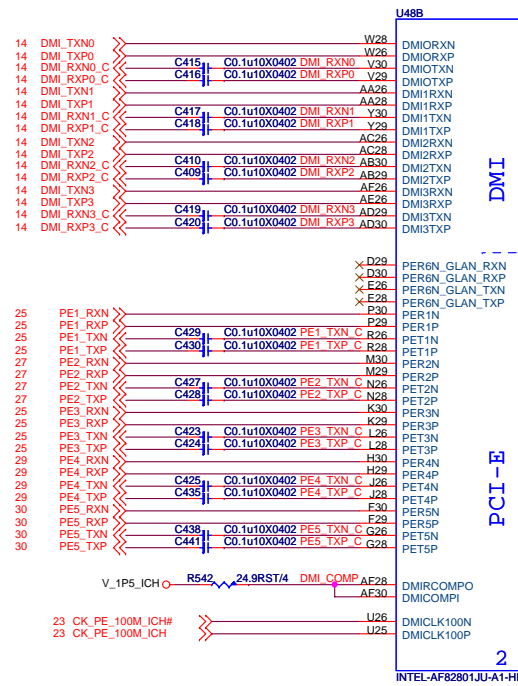
SINGLE\_IOH  
Used for dual TBG IOH selection:  
"0": IOH is not connected to another IOH on some CSI link (default)  
"1": IOH is connected to another IOH on some CSI link

CL\_CLK\_SRC  
Used for ME default clock source:  
"1": PLL (default) -- EXT ME CLK  
"0": Ring Oscillator (back-up) -- INT ME CLK



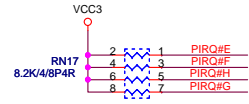


PE1 : X1 SLOT  
PE2 : LAN1  
PE3 : X1 SLOT  
PE4 : JMB361  
PE5 : SIL3123

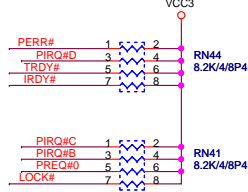
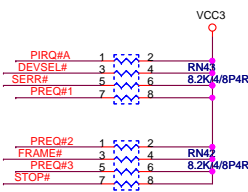


PCI-E

2 OF 6



## PCI PULL-UP / DOWN RESISTORS



## SB STRAPPING RESISTOR



BOOT SELECT STRAPS		
BOOT DEVICE	GNT#0	SPI_CS1#
LPC	1	1
SPI	0	1
PCI	1	0



SIGNAL	H	L	DES.
GNT3	DIS	EN	A16 OVERRIDE
GNT2	N/A	SET BIT	PCIE PORT CONFIG 2 BIT 0 (5-6)
GNT1	DC	AC	DMI AC/DC MODE 0 : AC 1 : DC

**MSI**  
Link to the Future

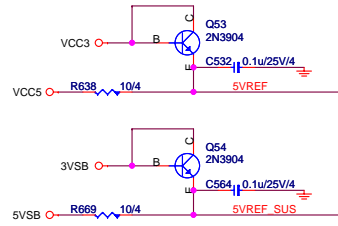
**MICRO-START INT'L CO.,LTD.**

Title: **ICH10 - PCI, USB, DMI, PCIE X1**

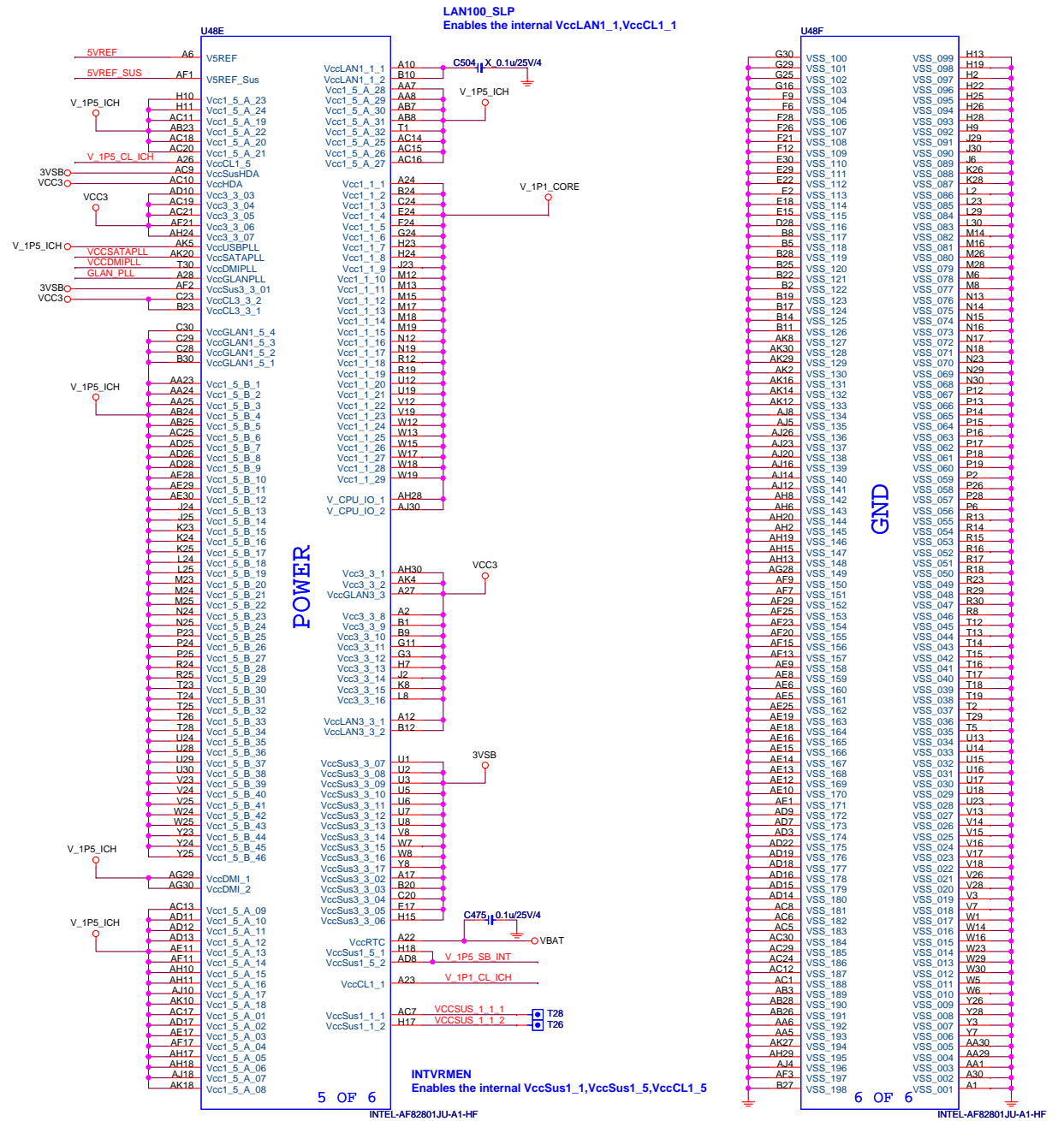
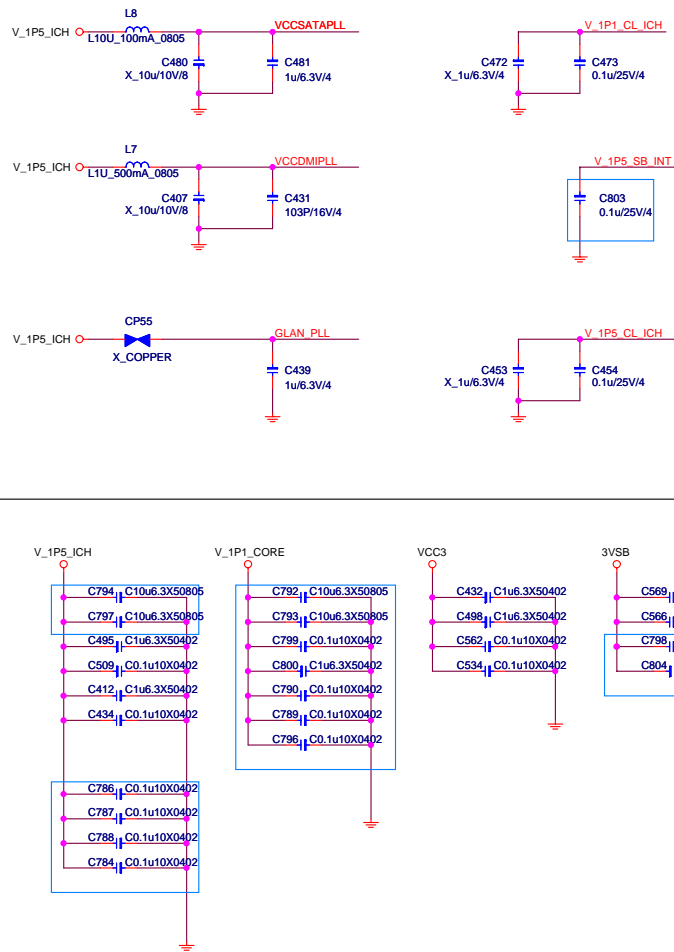
Size: Custom Document Number: **DELL Delmos** Rev: **0A**

Date: Friday, November 21, 2008 Sheet: 21 of 40

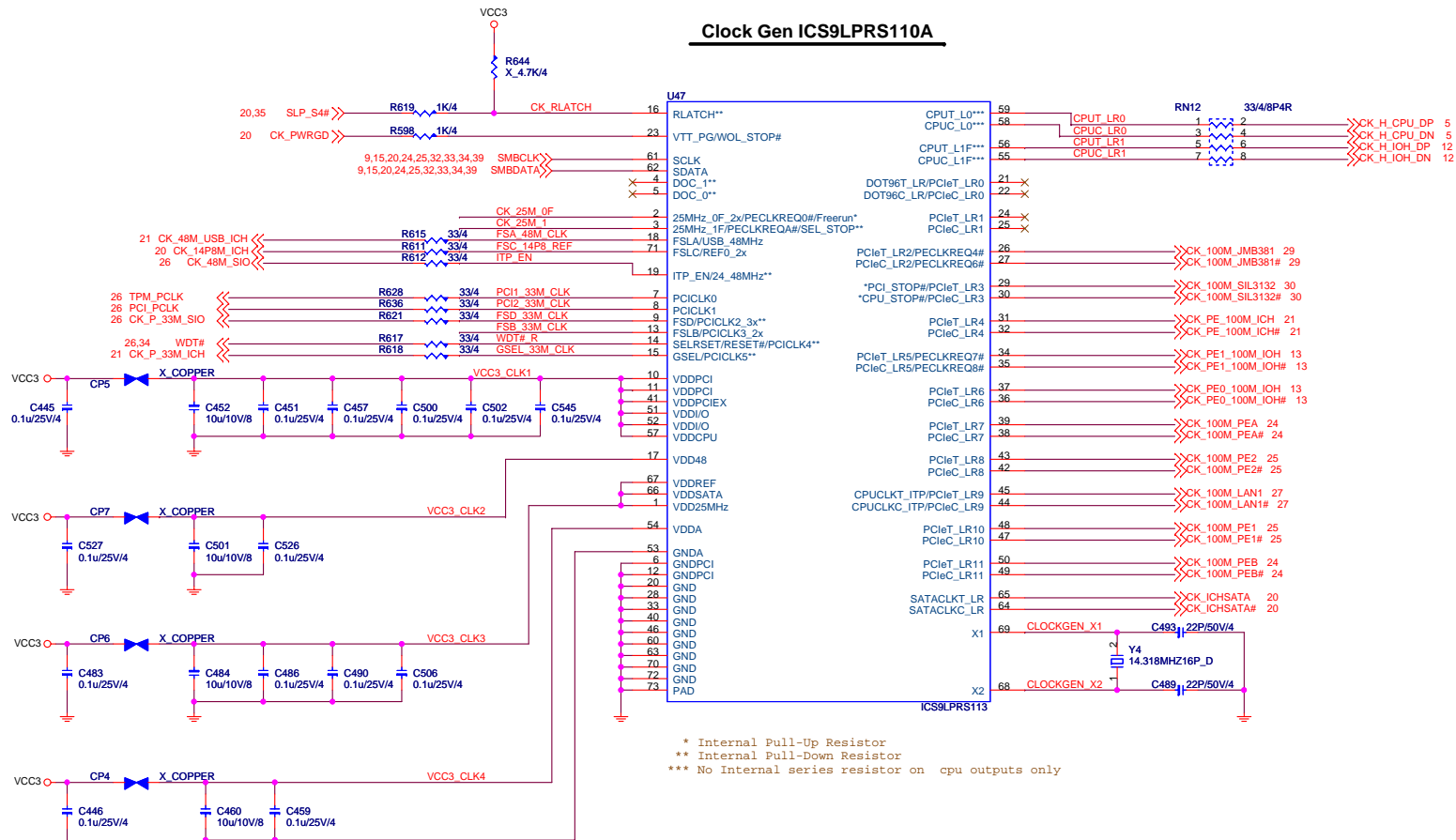
## 5VREF & 5VREF\_SUS Sequencing Circuit



## SB POWER



## Clock Gen ICS9LPRS110A



```
* Internal Pull-Up Resistor
** Internal Pull-Down Resistor
*** No Internal series resistor on  cpu outputs only
```

BSSEL			TABLE
2	1	0	FSB FREQUENCY
0	0	0	266 MHz
0	0	1	133 MHz ( default )
0	1	0	200 MHz
0	1	1	166 MHz
1	0	0	333 MHz
1	0	1	100 MHz
1	1	0	400 MHz
1	1	1	200 MHz

## CLOCK GEN STRAPING

0: Pin21/22 100MHz \* GSEL\_33M\_CLK R643 X 4.7K/4 VCC3  
1: Pin21/22 96MHz Internal pull down

0: PCICLK4  
1: RESET \*

WDT# R R642 4.7K/4 VCC3  
Internal pull down

0: PCIE\_X9\_\*  
1: CPU\_ITP

1 : 25MHz freerun function

Internal pull up

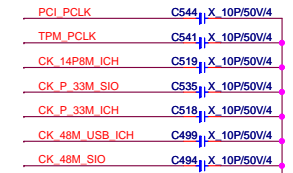
1 = Selects pin 29/30 to be PCI\_STOP#/CPU\_STOP#

For ICS CPU/DIV SEL

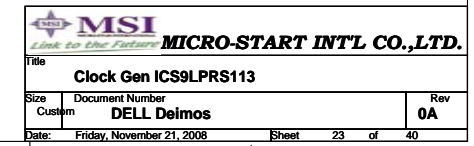
1: FSLD Bit3=1

FSD 33M CLR R631 4.7K/4

Internal pull up

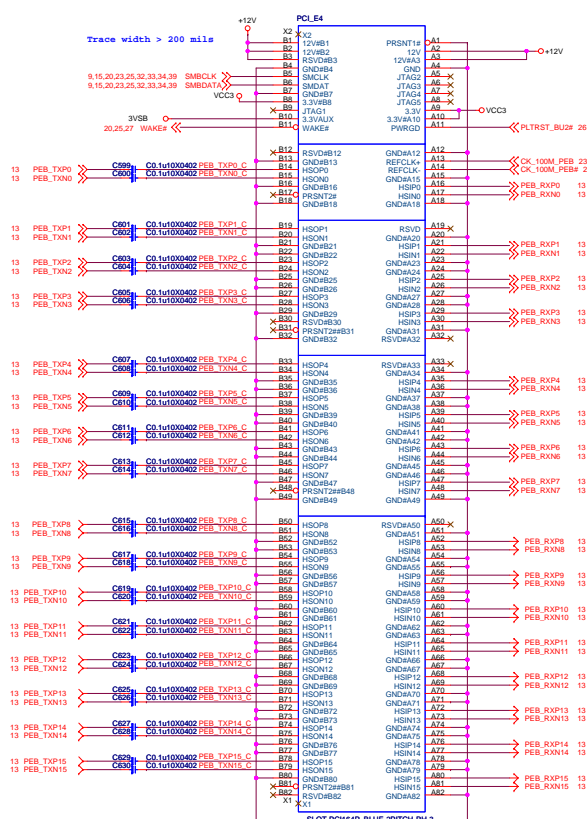
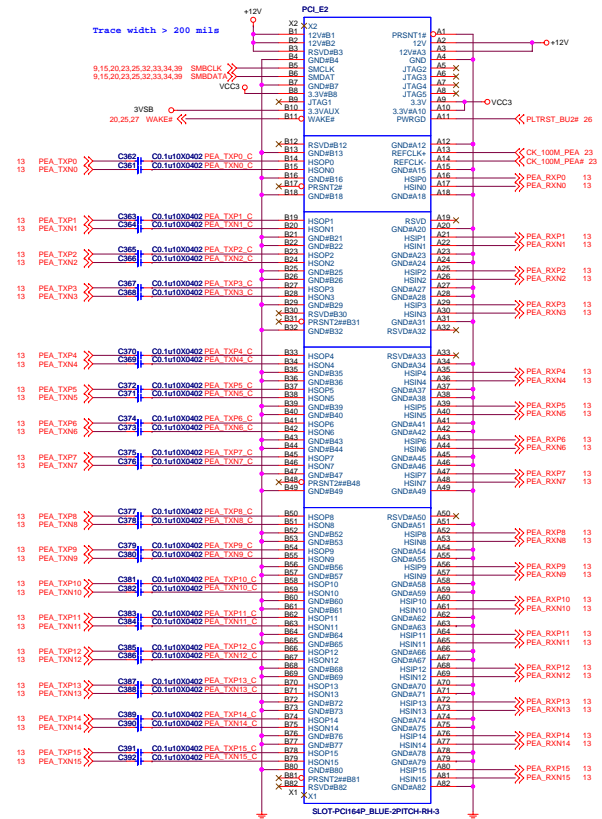


V\_1P1\_CORE

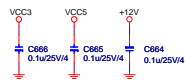
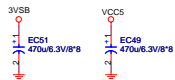
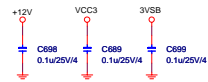
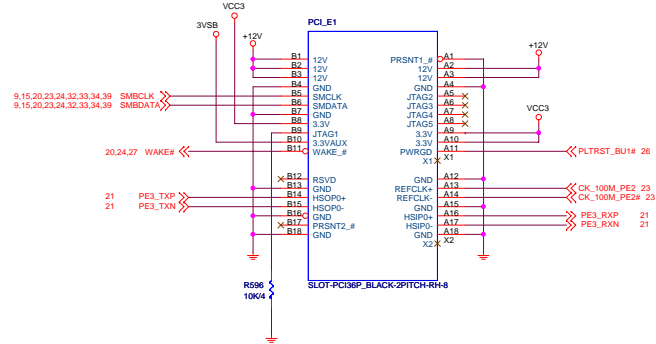
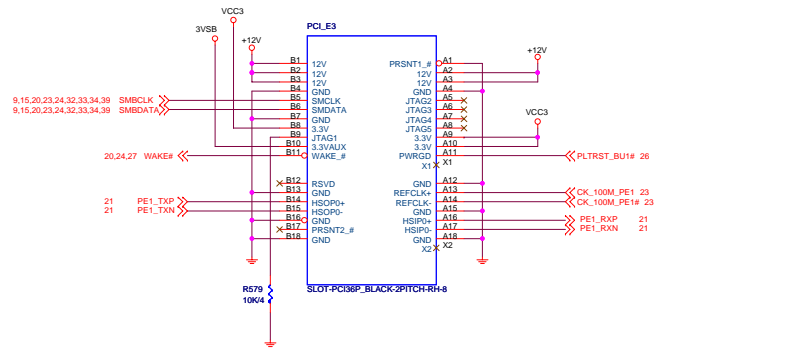


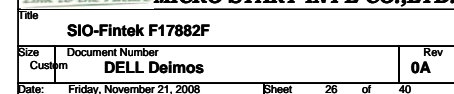


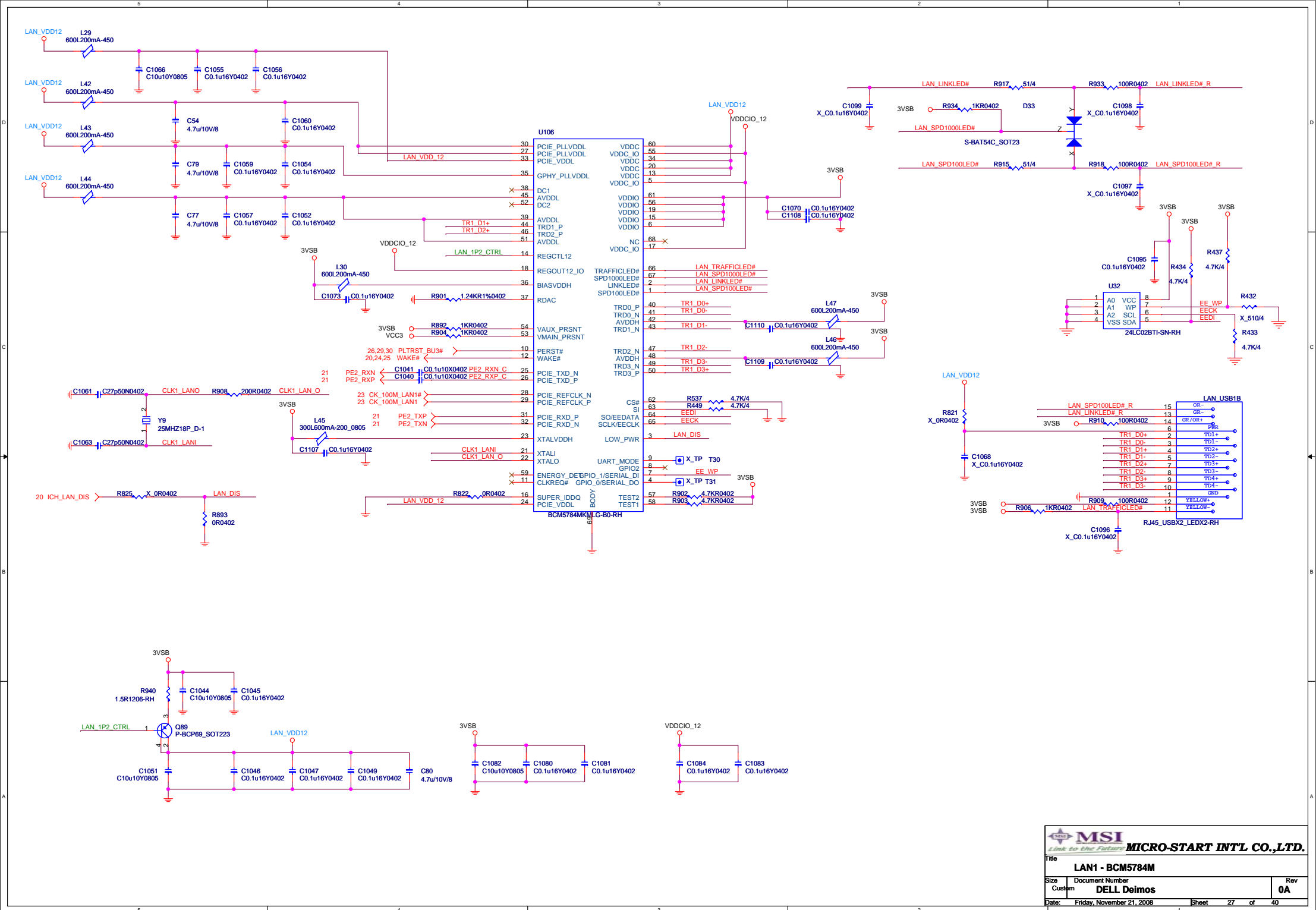
# PCI Express X16 SLOT1,2

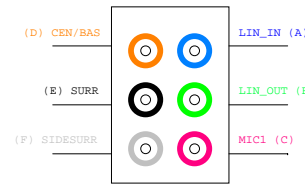
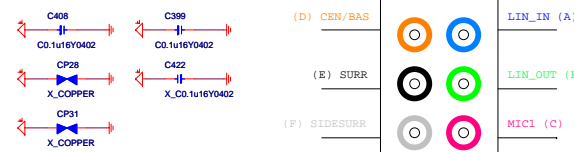
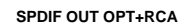
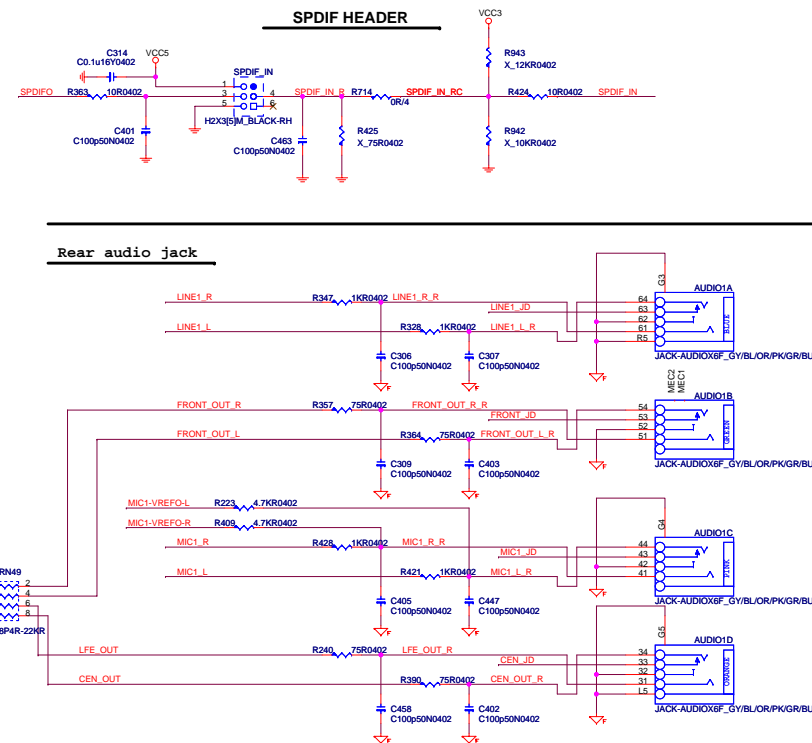




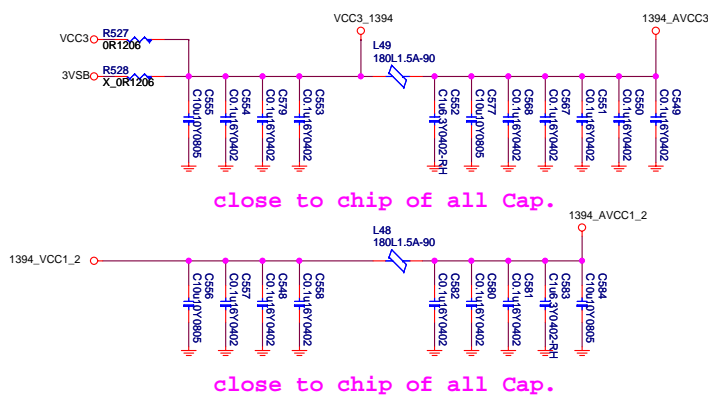
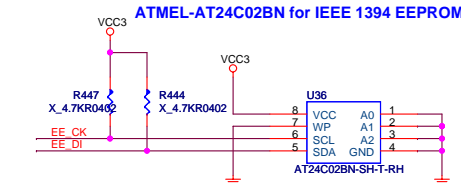
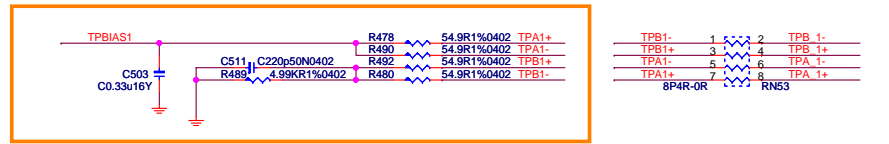
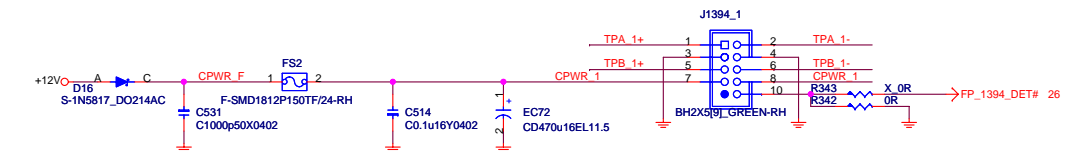
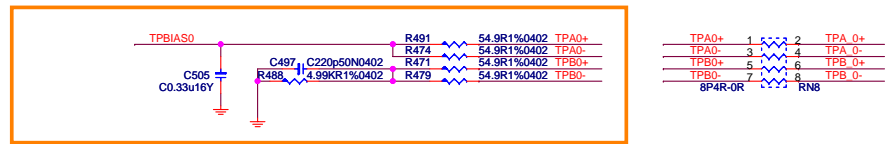
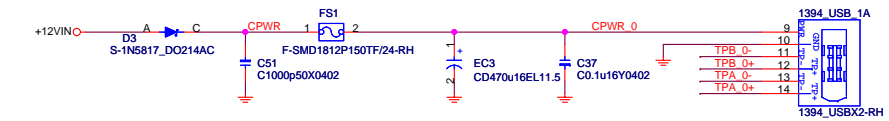









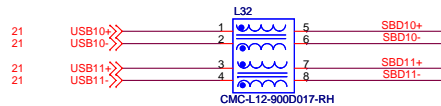
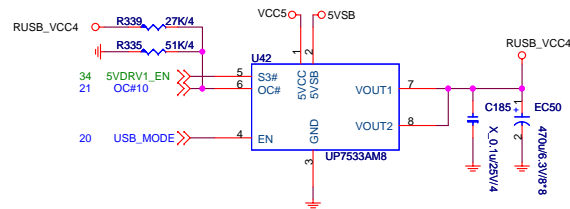
POWER



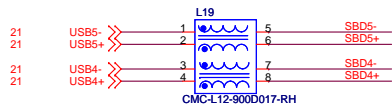
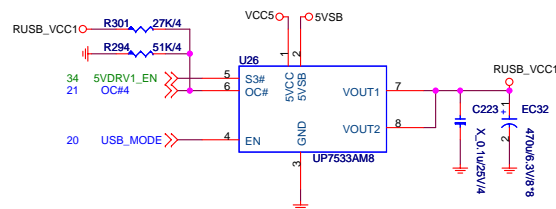
 <b>MSI</b> <i>Link to the Future</i>				<b>MICRO-START INT'L CO.,LTD.</b>			
<b>Title</b> <b>1394 Controller - VT6315N</b>							
<b>Size</b> <b>Custom</b>		<b>Document Number</b> <b>DELL Delmos</b>				<b>Rev</b> <b>0A</b>	
<b>Date:</b> Friday, November 21, 2008				<b>Sheet</b> 29		<b>of</b> 40	



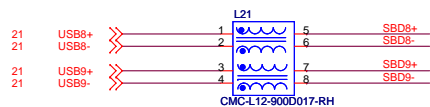
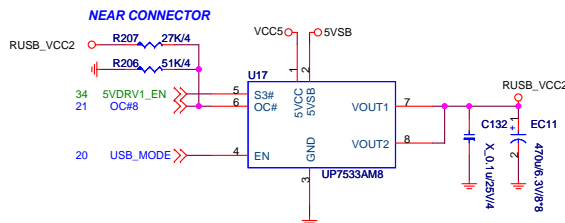
## USB POWER FOR PORT 10,11



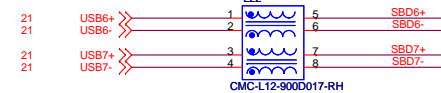
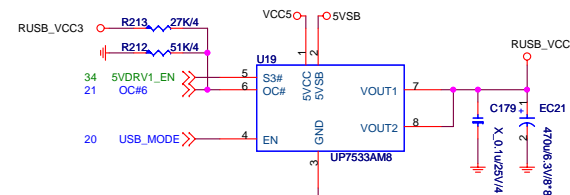
## REAR USB PORT 4,5 (With LAN)



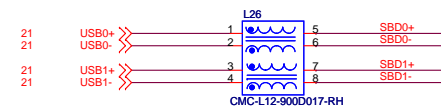
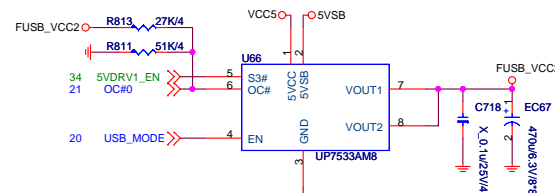
## Rear USB PORT 8,9 (With 1394)



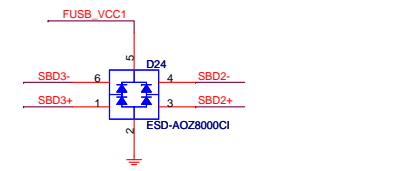
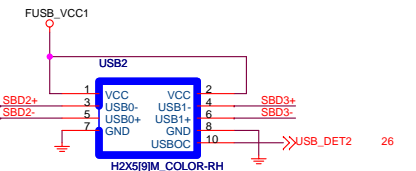
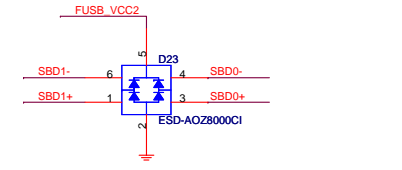
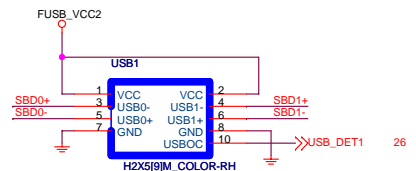
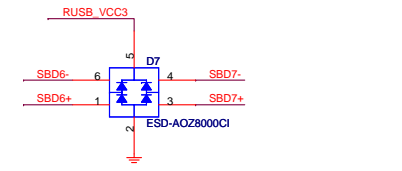
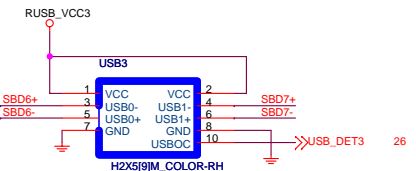
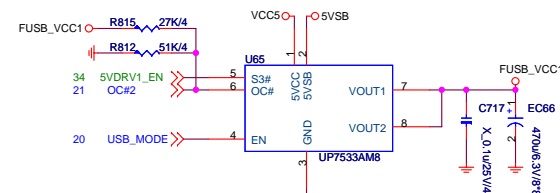
## USB POWER FOR PORT 6,7



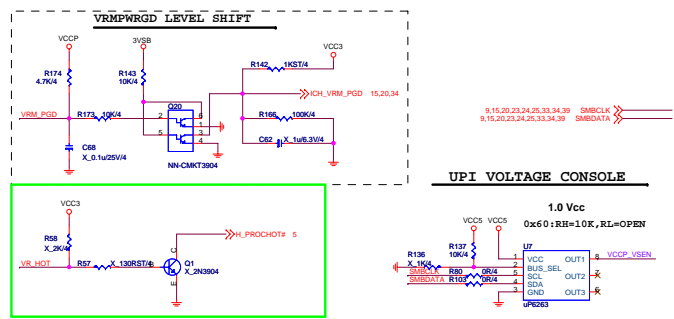
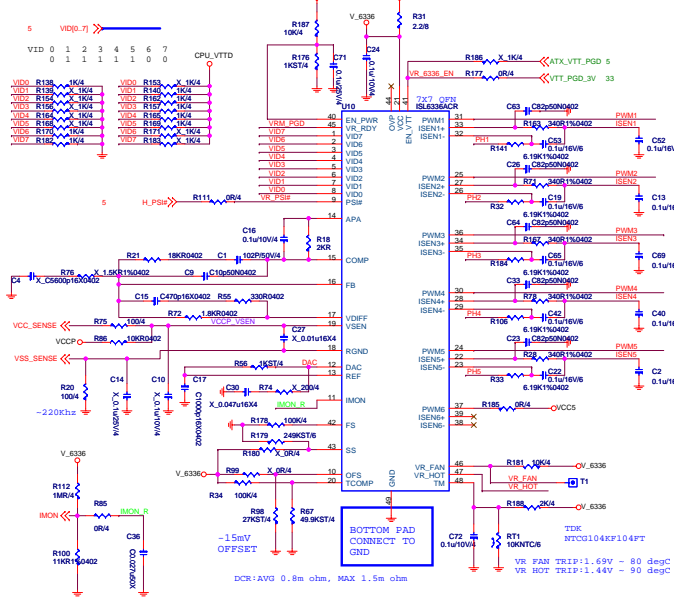
## USB POWER FOR PORT 0,1



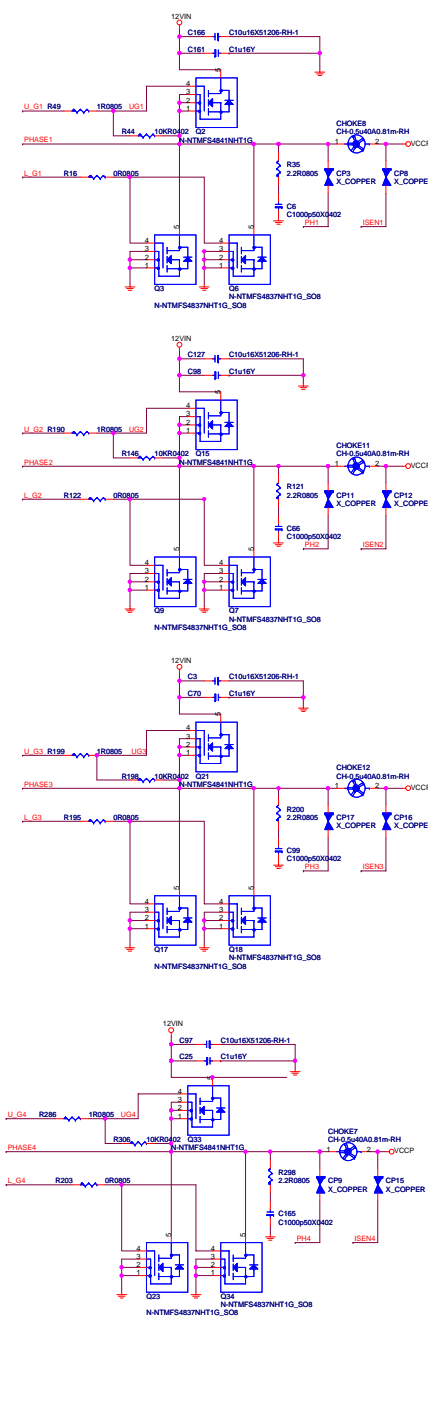
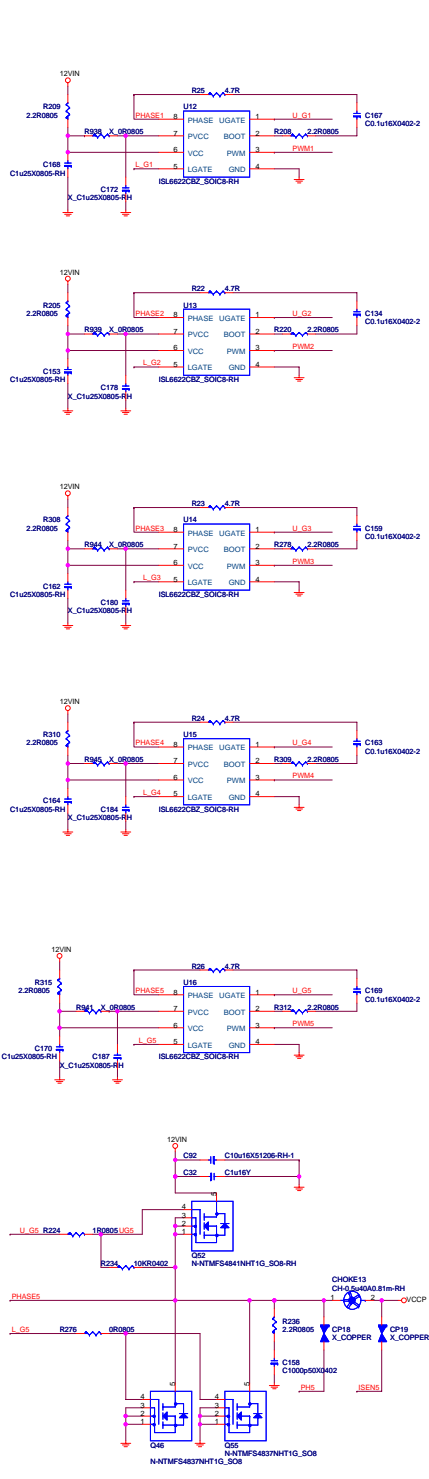
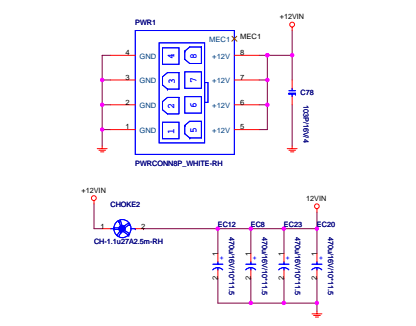
## USB POWER FOR PORT 8,9



ISL6336CR VRD11.1 POWER CKT

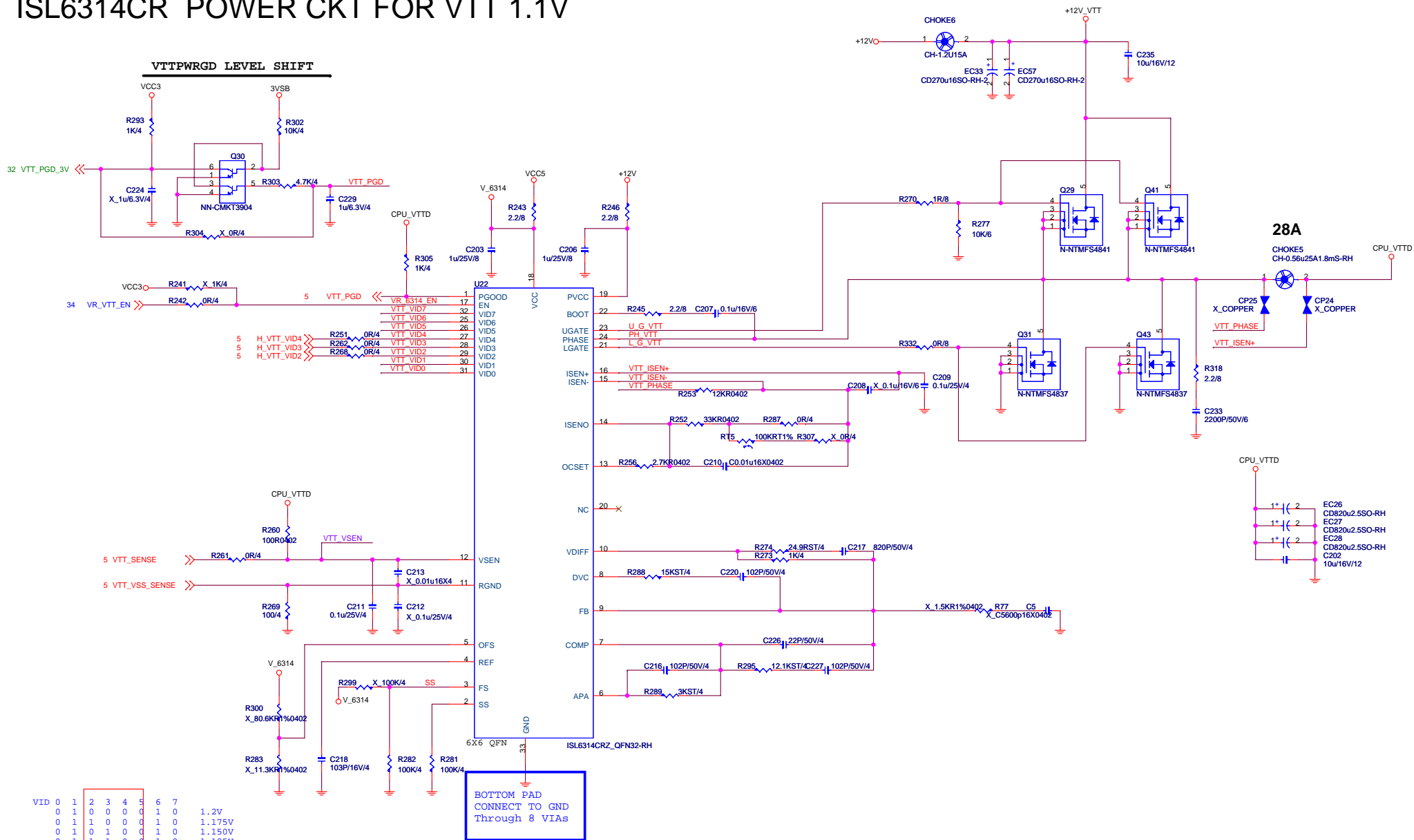


CPU +12VIN POWER CONN.





## ISL6314CR POWER CKT FOR VTT 1.1V

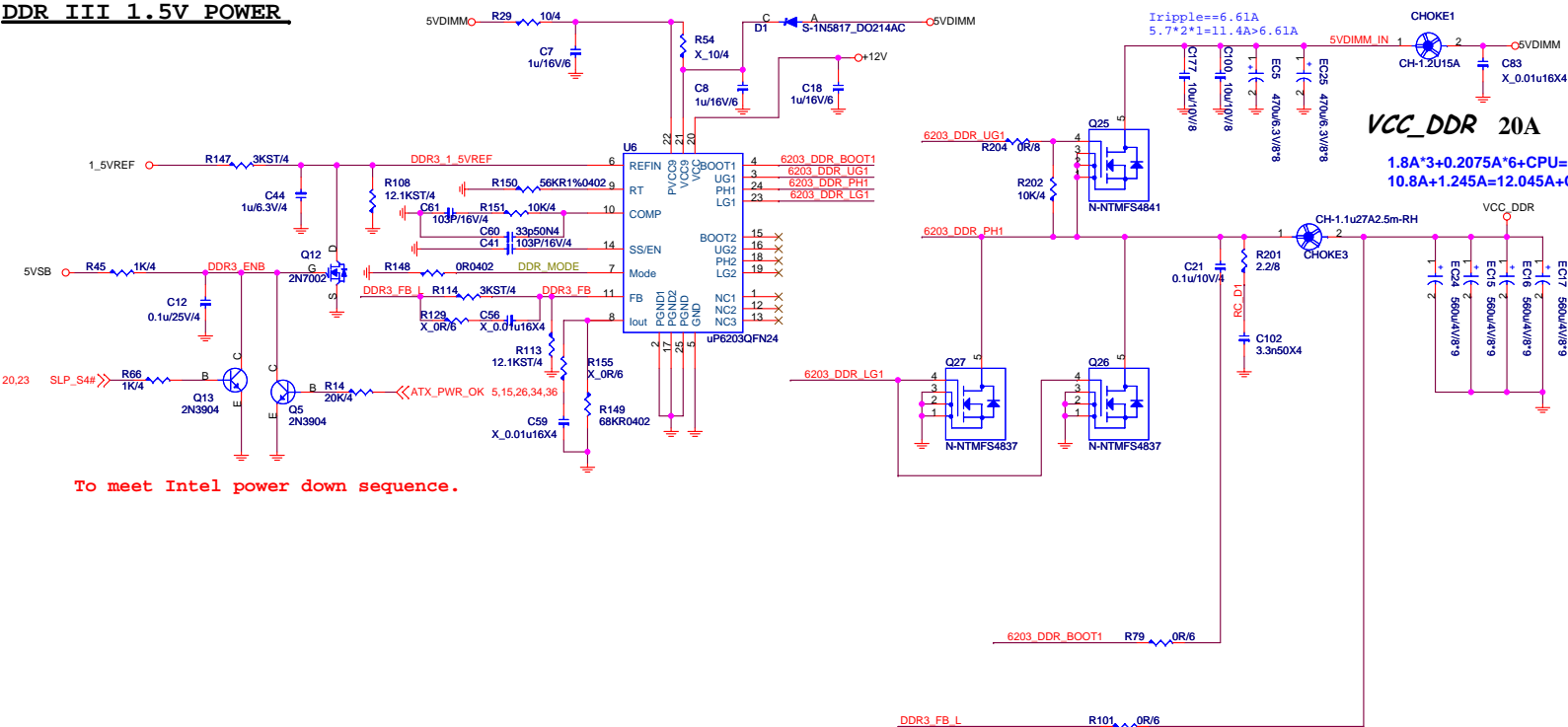


## UPI VOLTAGE CONSOLE



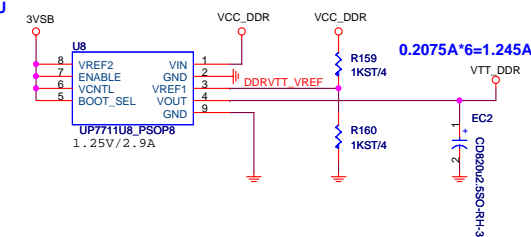


## DDR III 1.5V POWER

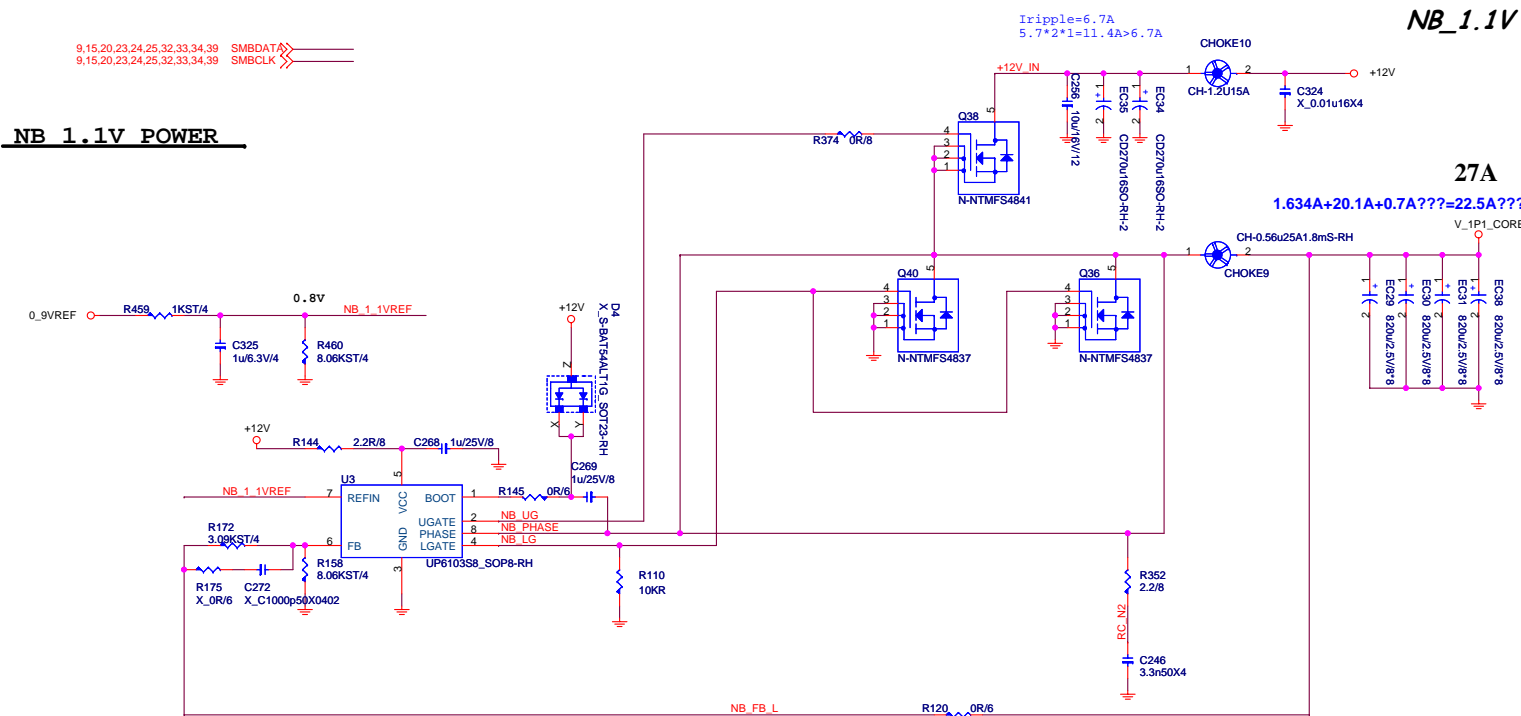


### DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .

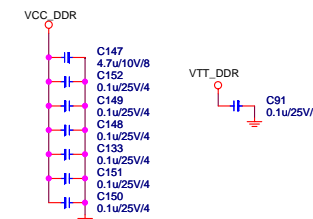


NB 1.1V POWER

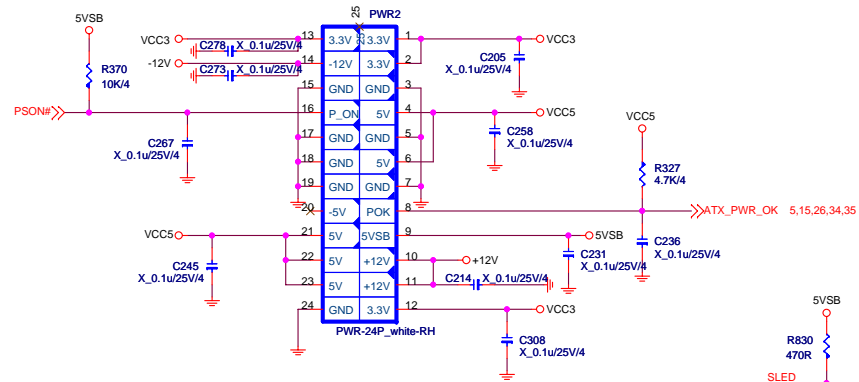


***NB\_1.1V***

**27A**  
1.634A+20.1A+0.7A???=22.5A???



## ATX POWER CONNECTOR

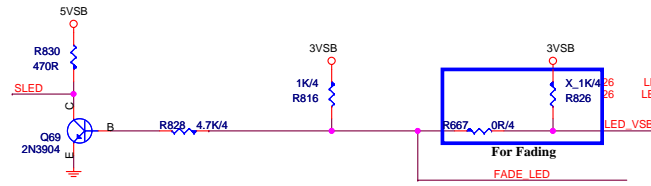


## FRONT PANNEL LED Control Circuit

No Support Fading Function

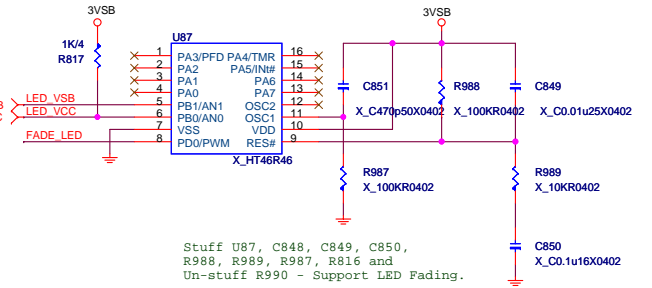
	LED_VCC	LED_VSB	PLED	SLED
S5, S4	H	H	L	L
S1, S3	L	H & L	L	H & L
S0	H	L	L	H
No Post	H	H	H	L

LED ( By Fintek 71882)



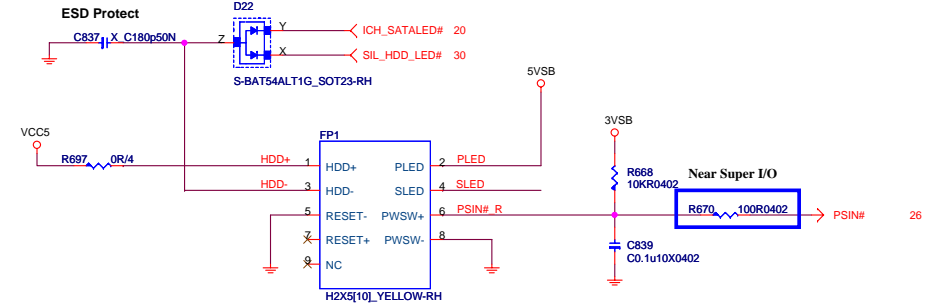
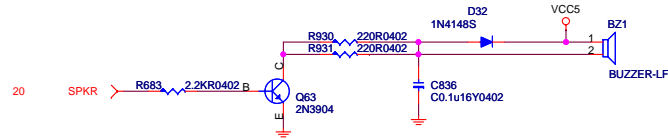
Support Fading Function

	LED_VSB	LED_VCC	FADE_LED	PLED	SLED
S0	L	L	L	L	H
S1, S3	H	L	Fading	L	Fading
S4, S5	L	H	H	L	L
No Post	H	H	H	H	L



Stuff U87, C848, C849, C850, R988, R989, R987, R816 and Un-stuff R990 - Support LED Fading.

Un-stuff U87, C848, C849, C850, R988, R989, R987, R816 and Stuff R990 - No LED Fading Function.



The image displays three wiring diagrams for SATA ports (SATA1, SATA2, and SATA3) connected to a SATA14PM\_Purple-RH connector. Each diagram shows the connection between a SATA port and a SATA14PM\_Purple-RH connector. The diagrams include pin numbers, component labels, and signal names.

**SATA1 Diagram:**

- Left Side (SATA1):**
  - Pin 1: GND
  - Pin 2: HT+1
  - Pin 3: HT-1
  - Pin 4: GND
  - Pin 5: HR-1
  - Pin 6: HR+1
  - Pin 7: GND
  - Pin 8: MEC1MEC2
- Right Side (SATA14PM\_Purple-RH):**
  - Pin 8: ST TX1
  - Pin 9: ST TX#1
  - Pin 10: ST RX#1
  - Pin 11: ST RX#1
  - Pin 12: ST RX#1
  - Pin 13: ST RX#1
  - Pin 14: ST RX#1
  - Pin 15: ST RX#1
  - Pin 16: ST RX#1

**SATA2 Diagram:**

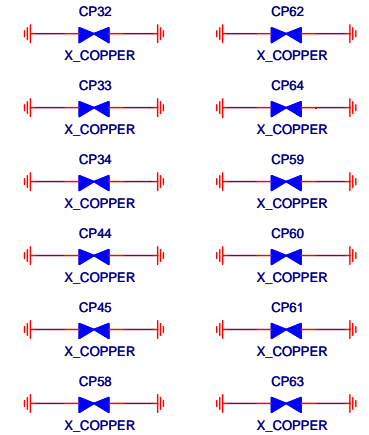
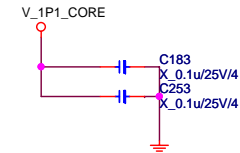
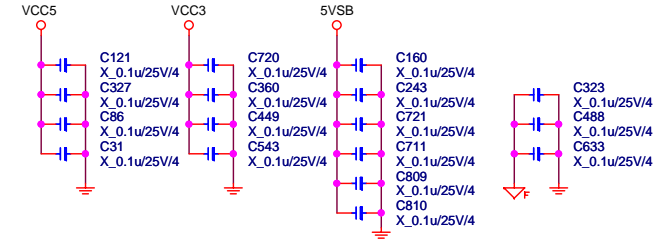
- Left Side (SATA2):**
  - Pin 1: GND
  - Pin 2: HT+1
  - Pin 3: HT-1
  - Pin 4: GND
  - Pin 5: HR-1
  - Pin 6: HR+1
  - Pin 7: GND
  - Pin 8: MEC1MEC2
- Right Side (SATA2):**
  - Pin 8: ST TX2
  - Pin 9: ST TX#2
  - Pin 10: ST RX#2
  - Pin 11: ST RX#2
  - Pin 12: ST RX#2
  - Pin 13: ST RX#2
  - Pin 14: ST RX#2
  - Pin 15: ST RX#2
  - Pin 16: ST RX#2

**SATA3 Diagram:**

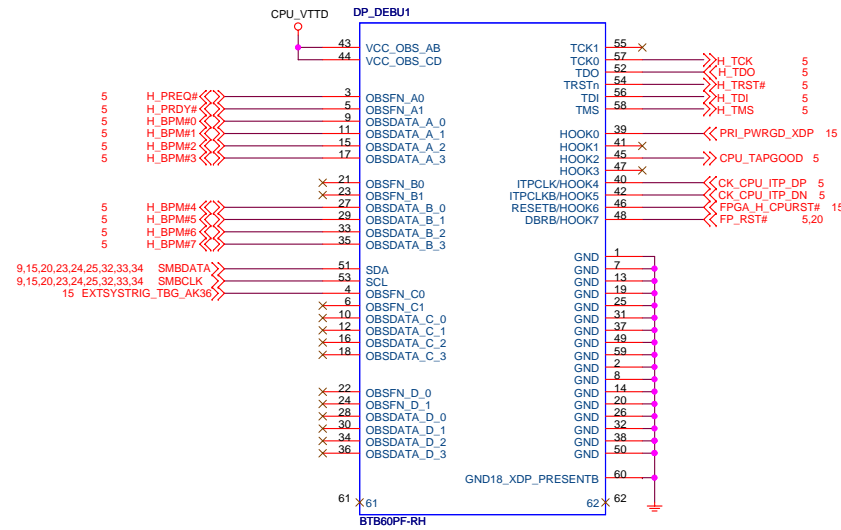
- Left Side (SATA3):**
  - Pin 1: GND
  - Pin 2: HT+1
  - Pin 3: HT-1
  - Pin 4: GND
  - Pin 5: HR-1
  - Pin 6: HR+1
  - Pin 7: GND
  - Pin 8: MEC1MEC2
- Right Side (SATA3):**
  - Pin 8: ST TX3
  - Pin 9: ST TX#3
  - Pin 10: ST RX#3
  - Pin 11: ST RX#3
  - Pin 12: ST RX#3
  - Pin 13: ST RX#3
  - Pin 14: ST RX#3
  - Pin 15: ST RX#3
  - Pin 16: ST RX#3

[illegible][illegible]

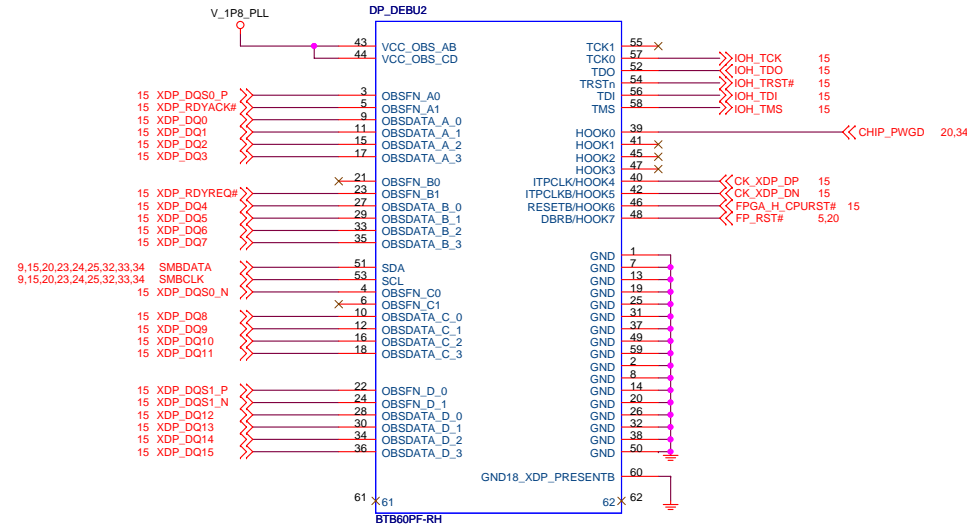
## EMI CAP



# Reserve debug port 5020

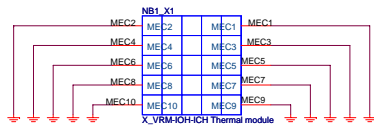


# Reserve debug port 5020





PF0-075910A~G37  
PF0-075910A~T53



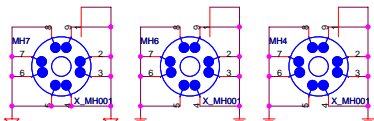
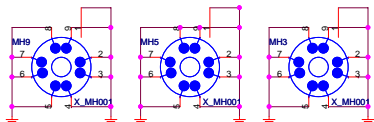
### Optical Fiducial Marks-120



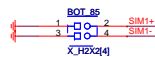
### Optical Fiducial Marks-100



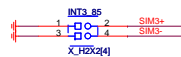
### Mounting Holes



5/5 85 ohm



5/7 85 ohm



Title		
Manual Parts		
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